

Features

- Single chip solution with only a few external components
- Stand-alone fixed-frequency user mode
- Programmable multi-channel user mode
- Low current consumption in active mode and very low standby current
- PLL-stabilized RF VCO (LO) with internal varactor diode
- Lock detect output in programmable user mode
- On-chip AFC for extended input frequency acceptance range
- 3wire bus serial control interface
- FSK/ASK mode selection
- FSK for digital data or FM for analog signal reception
- RSSI output for signal strength indication and ASK reception
- ASK detection normal or with peak detector
- Switchable LNA gain for improved dynamic range
- Automatic PA turn-on after PLL lock
- ASK modulation achieved by PA on/off keying
- 32-pin Micro Leadframe Package Quad (MLPQ 5x5)

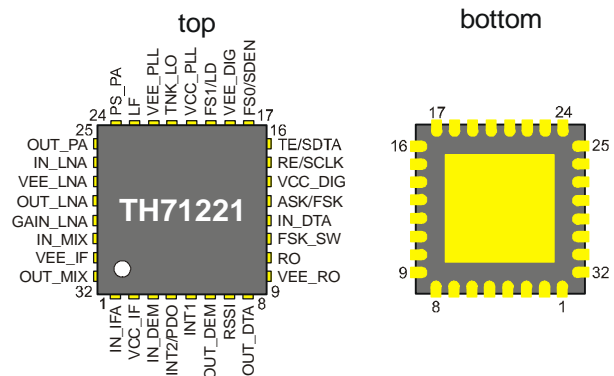
Ordering Information

Part No.	Temperature Code	Package Code
TH71221	E (-40 °C to 85 °C)	LQC (32L MLPQ 5x5)

Application Examples

- General bi-directional half duplex digital data RF signaling or analog signal communication
- Low-power telemetry
- Alarm and security systems
- Remote Keyless Entry (RKE)
- Tire Pressure Monitoring System (TPMS)
- Garage door openers
- Intelligent remote control
- Home automation

Pin Description



General Description

The TH71221 is a single chip FSK/FM/ASK transceiver IC. It is designed to operate in low-power multi-channel programmable or single-channel stand-alone, half-duplex data transmission systems. It can be used for ISM, SRD or any other application operating in the frequency ranging of 300 MHz to 930 MHz. In programmable user mode, the transceiver can operate down to 27 MHz by employing an external VCO varactor diode.

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1 Theory of Operation

1.1 General

The main building block of the transceiver is a programmable PLL frequency synthesizer that is based on an integer-N topology. The PLL is used for generating the carrier frequency during transmission and for generating the LO signal during reception. The carrier frequency can be FSK-modulated by pulling the crystal and ASK-modulated by on/off keying of the power amplifier. The receiver is based on the principle of a single conversion superhet. Therefore the VCO frequency has to be changed between transmit and receive mode. In receive mode, the preferred LO injection type is low-side injection.

The TH71221 transceiver IC consists of the following building blocks:

- Low-noise amplifier (LNA) for high-sensitivity RF signal reception with switchable gain
- Mixer (MIX) for RF-to-IF down-conversion
- IF amplifier (IFA) to amplify and limit the IF signal and for RSSI generation
- Phase-coincidence demodulator with external ceramic discriminator (FSK Demodulator)
- Operational amplifier (OA1), connected to demodulator output
- Operational amplifier (OA2), for general use
- Peak detector (PKDET) for ASK detection
- Control logic with 3wire bus serial control interface (SCI)
- Reference oscillator (RO) with external crystal
- Reference divider (R counter)
- Programmable divider (N/A counter)
- Phase-frequency detector (PFD)
- Charge pump (CP)
- Voltage controlled oscillator (VCO) with internal varactor
- Power amplifier (PA) with adjustable output power

1.2 Technical Data Overview

- ❑ Frequency range: 300 MHz to 930 MHz in programmable user mode
- ❑ Extended frequency range with external VCO varactor diode: 27 MHz to 930 MHz
- ❑ 315 MHz, 433 MHz, 868 MHz or 915 MHz fixed-frequency settings in stand-alone user mode
- ❑ Power supply range: 2.2 V to 5.5 V
- ❑ Temperature range: -40 °C to +85 °C
- ❑ Standby current: 50 nA
- ❑ Operating current: 6.5 mA in receive mode at low gain
- ❑ Operating current 12 mA in transmit mode at -2 dBm output power
- ❑ Adjustable output power range from -20 dBm to +10 dBm
- ❑ Sensitivity: -105 dBm at FSK with 150 kHz IF filter BW
- ❑ Sensitivity: -107 dBm at ASK with 150 kHz IF filter BW
- ❑ Max. data rate with crystal pulling: 20 kbps NRZ
- ❑ Max. data rate with direct VCO modulation: 115 kbps NRZ
- ❑ Max. input level: -10 dBm at FSK and -20 dBm at ASK
- ❑ Input frequency acceptance: ± 10 to ± 150 kHz (depending on FSK deviation)
- ❑ Frequency deviation range: ± 2.5 to ± 80 kHz
- ❑ Analog modulation frequency: max. 10 kHz
- ❑ Crystal reference frequency: 3 MHz to 12 MHz
- ❑ External reference frequency: 1 MHz to 16 MHz

1.3 Note on ASK Modulation

The TH71221 can be used over the full operating frequency range in ASK receive mode. In ASK transmit mode the max. operating frequency should not exceed 450 MHz, and the max. output power should not exceed 3 dBm. For best results, a large PFD frequency should be used. An external ASK modulator can be used for higher frequencies and/or higher power levels.

1.4 Block Diagram

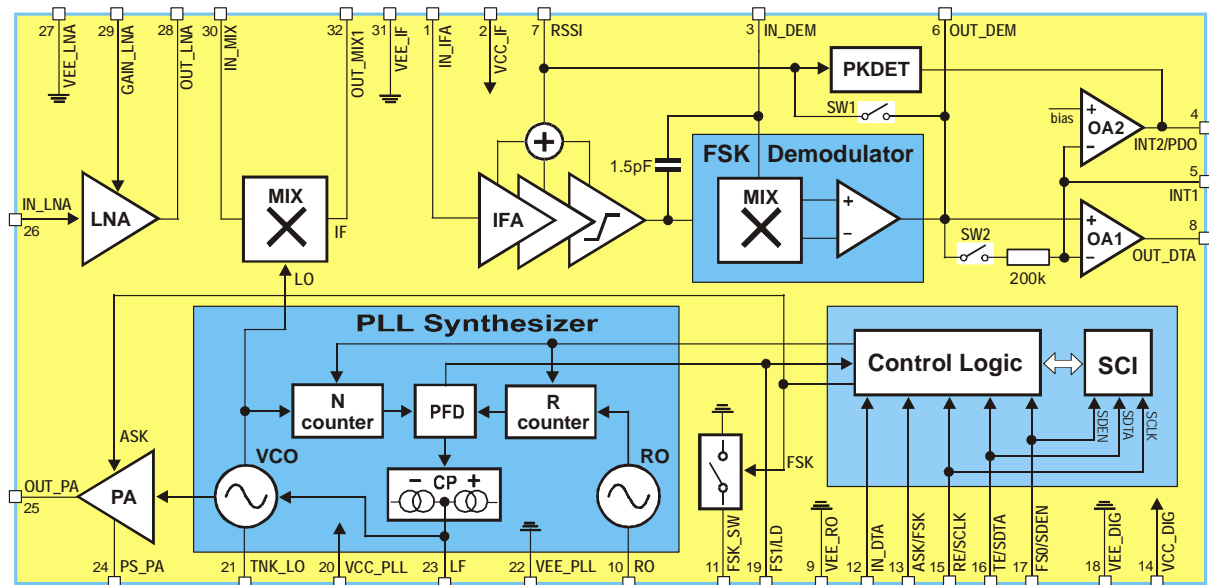


Fig. 1: TH71221 block diagram

1.5 User Mode Features

The transceiver can operate in two different user modes. It can be used either as a 3-wire-bus-controlled programmable or as a stand-alone fixed-frequency device. After power up, the transceiver is set to fixed-frequency mode – the Stand-alone User Mode (SUM). In this mode, pins FS0/SDEN and FS1/LD must be connected to V_{EE} or V_{CC} in order to set the desired frequency of operation. The logic levels at pins FS0/SDEN and FS1/LD must not be changed after power up in order to remain in fixed-frequency mode. After the first logic level change at pin FS0/SDEN, the transceiver enters into Programmable User Mode (PUM) while pin FS1/LD is now a PLL lock detector output. In this mode, the user can set any PLL frequency or mode of operation by the SCI. In SUM pins FS0/SDEN and FS1/LD are used to set the desired frequency, while in PUM pin FS0/SDEN is part of the 3-wire serial control interface (SCI) and pin FS1/LD is the lock detector output signal of the PLL synthesizer.

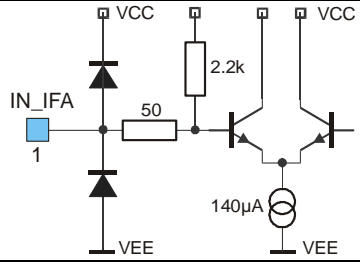
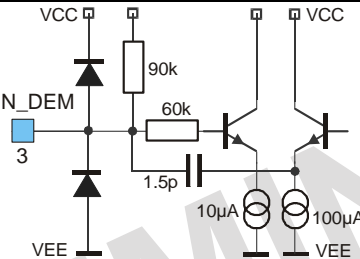
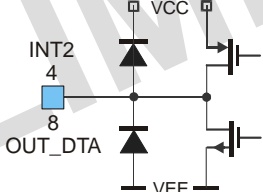
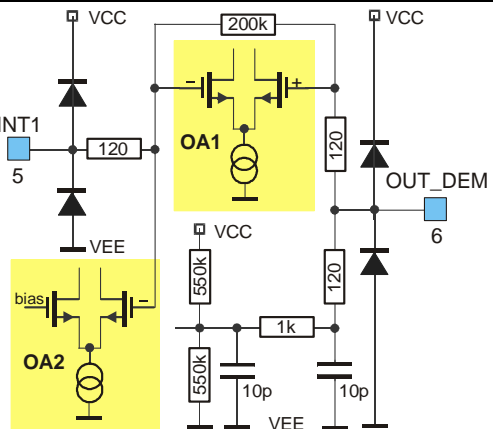
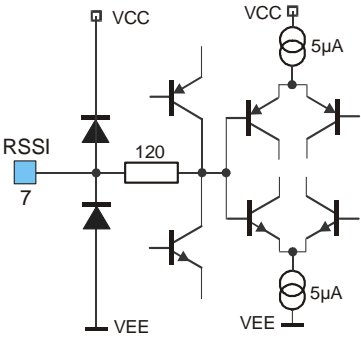
The following four fixed-frequency settings can be selected in SUM:

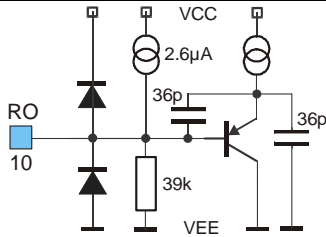
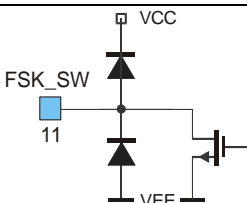
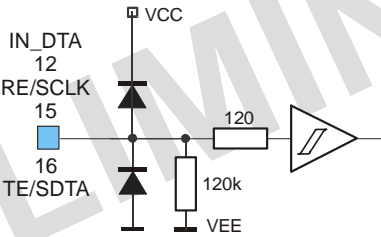
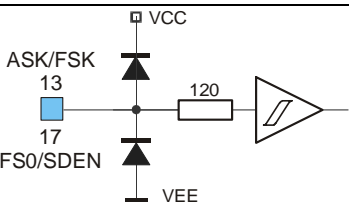
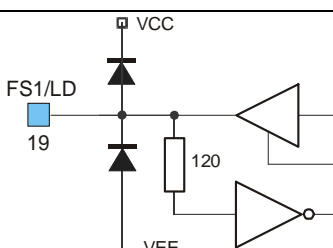
Channel frequency	433.92 MHz	868.3 MHz	315 MHz	915 MHz
Please refer to para. 4 for detailed information.				

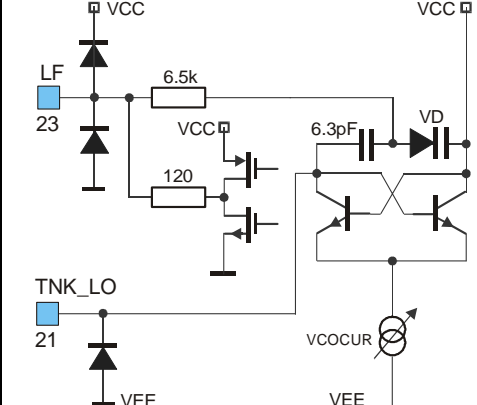
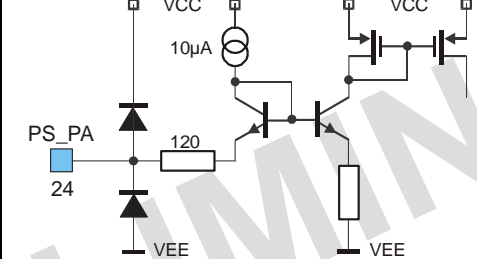
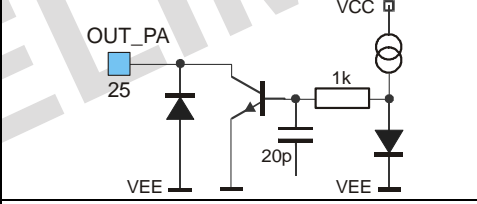
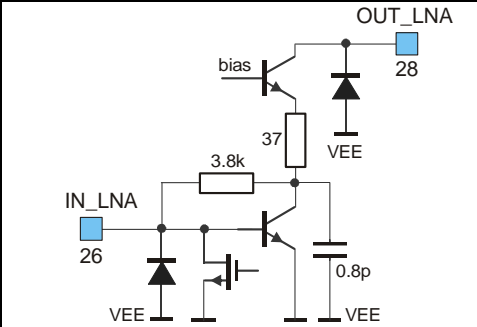
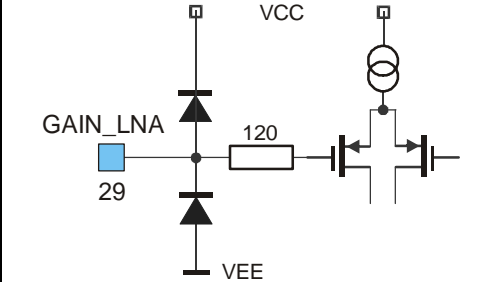
A mode control logic allows four different operational modes. In addition to standby, transmit and receive mode, idle mode can be used to run only the reference oscillator and the PLL. The different operational modes can be set in SUM and PUM as well. In SUM, the user can set the transceiver operational modes via control pins RE/SCLK and TE/SDTA, please refer to para. 4 for detailed information.

The register bits OPMODE select the desired operation mode in PUM. It should be noted that the pin notification RE/SCLK and TE/SDTA describes the modes Receive Enable and Transmit Enable in SUM. These pins are part of the 3-wire SCI during PUM.

2 Pin Definitions and Descriptions

Pin No.	Name	I/O Type	Functional Schematic	Description
1	IN_IFA	input		IF amplifier input, approx. 2 kΩ single-ended
2	VCC_IF	supply		positive supply of LNA, MIX, IFA, FSK Demodulator, PA, OA1 and OA2
3	IN_DEM	analog I/O		IF amplifier output and demodulator input, connection to external ceramic discriminator
4	INT2/PDO	output		OA2 output or peak detector output
8	OUT_DTA	output		OA1 output
5	INT1	input		inverting inputs of OA1 and OA2
6	OUT_DEM	analog I/O		demodulator output and non-inverting OA1 input
7	RSSI	output		RSSI output

Pin No.	Name	I/O Type	Functional Schematic	Description
9	VEE_RO	ground		ground of RO
10	RO	analog I/O		RO input, base of bipolar transistor
11	FSK_SW	analog I/O		FSK pulling pin, switch to ground or OPEN
12	IN_DTA	input		ASK/FSK modulation data input, pull down resistor 120kΩ
15	RE/SCLK	input		receiver enable input / clock input for the shift register, pull down resistor 120kΩ
16	TE/SDTA	input		transmitter enable input / serial data input, pull down resistor 120kΩ
13	ASK/FSK	input		ASK/FSK mode select input
17	FS0/SDEN	input		frequency select input / serial data enable input
14	VCC_DIG	supply		positive supply of serial port and control logic
18	VEE_DIG	ground		ground of serial port and control logic
19	FS1/LD	input		frequency select input / lock detector output
20	VCC_PLL	supply		positive supply of PLL frequency synthesizer
22	VEE_PLL	ground		ground of PLL frequency synthesizer

Pin No.	Name	I/O Type	Functional Schematic	Description
23	LF	analog I/O		charge pump output, connection to external loop filter
21	TNK_LO	analog I/O		VCO open-collector output, connection to external LC tank
24	PS_PA	analog I/O		power-setting input
25	OUT_PA	output		power amplifier open-collector output
27	VEE_LNA	ground		ground of LNA and PA
28	OUT_LNA	output		LNA open-collector output, connection to external LC tank at RF
26	IN_LNA	input		LNA input, single-ended
29	GAIN_LNA	input		LNA gain control input Low gain pin connected to V _{CC} High gain pin connected to GND

Pin No.	Name	I/O Type	Functional Schematic	Description
30	IN_MIX	input		mixer input, approx. 200Ω single-ended
31	VEE_IF	ground		ground of IFA, Demodulator, OA1 and OA2
32	OUT_MIX	output		mixer output, approx. 330Ω single-ended

Your Notes

PRELIMINARY

3 Functional Description

3.1 PLL Frequency Synthesizer

The TH71221 contains an integer-N PLL frequency synthesizer. A PLL circuit performs the frequency synthesis, via a feedback mechanism. The output frequency f_{VCO} is generated as an integer multiple of the phase detector comparison frequency f_R . This reference frequency f_R is generated by dividing the output frequency f_{RO} of a crystal oscillator. The phase detector utilizes this signal as a reference to tune the VCO and in the locked state it must be equal to the desired output frequency, divided by the feedback divider ratio N.

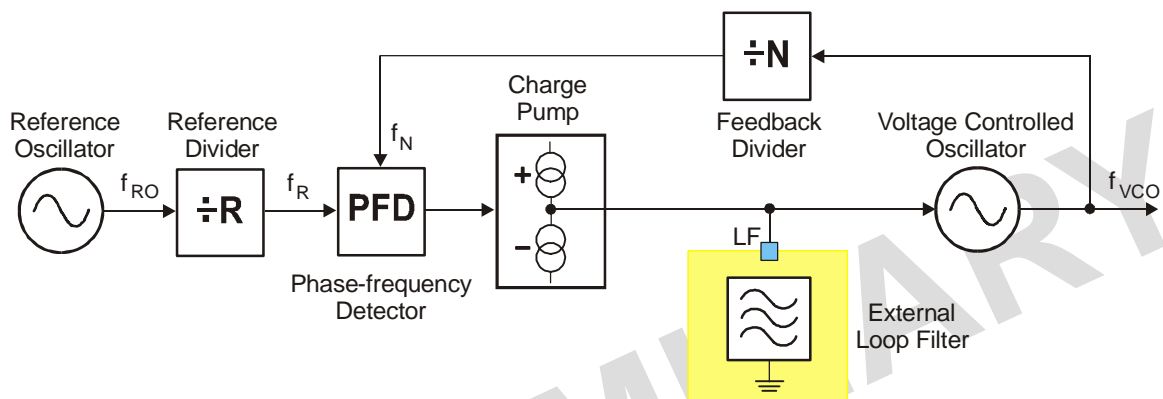


Fig. 2: Integer-N PLL Frequency Synthesizer Topology

The output frequency of the synthesizer f_{VCO} can be selected by programming the feedback divider and the reference divider. The only constraint for the frequency output of the system is that the minimum frequency resolution, or the channel spacing, must be equal to the PFD frequency f_R , which is given by the reference frequency f_{RO} and the reference divider factor R:

$$f_R = \frac{f_{RO}}{R}.$$

When the PLL is unlocked (e.g. during power up or during reprogramming of a new feedback divider ratio N), the phase-frequency detector PFD and the charge pump create an error signal proportional to the phase difference of the two input signals. This error signal is low-pass filtered through the external loop filter and input to the VCO to control its frequency. After the PLL has locked, the VCO frequency is given by the following equation:

$$f_{VCO} = N \frac{f_{RO}}{R}.$$

There are four registers available to set the VCO frequencies in receive (registers RR and NR) and in transmit mode (registers RT and NT). These registers can be programmed using the Serial Control Interface in the Programmable User Mode (PUM). In case of Stand-alone User Mode (SUM), the registers are set fixed values (refer to para. 4.1.1).

The VCO frequency is equal to the carrier frequency in transmit mode. While in receive mode the VCO frequency is offset by the intermediate frequency IF. This is because of the super-heterodyne nature of the receive part.

3.1.1 Reference Oscillator

The reference oscillator is based on a Colpitts topology with two integrated functional capacitors as shown in figure 3. The circuitry is optimized for a load capacitance range of 10 pF to 15 pF. The equivalent input capacitance C_{RO} offered by the oscillator input pin RO is about 18pF.

To ensure a fast and reliable start-up and a very stable frequency over the specified supply voltage and temperature range, the oscillator bias circuitry provides an amplitude regulation. The amplitude on pin RO is monitored in order to regulate the current of the oscillator core I_{RO} . There are two limits ROMAX and ROMIN between the regulation is maintained. These values can be changed via serial control interface in Programmable User Mode (PUM). In Stand-alone User Mode (SUM), ROMAX and ROMIN are set to default values (refer to para. 5.1.3). ROMAX defines the start-up current of the oscillator. The ROMIN value sets the desired steady-state current. If ROMIN is sufficient to achieve an amplitude of about 400 mV on pin RO, the current I_{RO} will be set to ROMIN. Otherwise the current will be permanently regulated between ROMIN and ROMAX. If ROMIN and ROMAX are equal, no regulation takes place. For most of the applications ROMIN and ROMAX should not be changed from default.

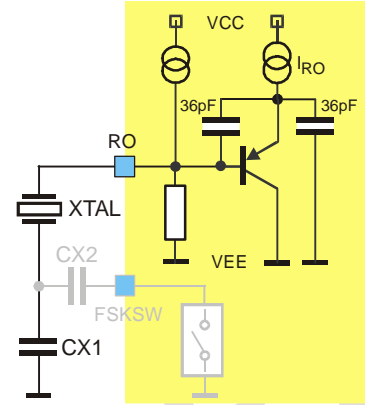


Fig. 3: Reference oscillator circuit

3.1.2 Reference Divider

The reference divider provides the input signal of the phase detector by dividing the signal of the reference oscillator. The ratio of the reference divider ranged is

$$4 \leq R \leq 1023,$$

3.1.3 Feedback Divider

The feedback divider of the PLL is based on a pulse-swallow topology. It contains a 4-bit swallow A-counter, a 13-bit program B-counter and a prescaler. The divider ratio of the prescaler is controlled by the program counter and the swallow counter. During one cycle, the prescaler divides by 17 until the swallow A-counter reaches its terminal count. Afterwards the prescaler divides by 16 until the program counter reaches its terminal count. Therefore the overall feedback divider ratio can be expressed as:

$$N = 17 \cdot A + 16 \cdot (B - A).$$

The A-counter configuration represents the lower bits in the feedback divider register ($N_{0-3} = A_{0-3}$) and the upper bits the B-counter configuration ($N_{4-16} = B_{0-12}$) respectively. According to that, the following counter ranges are implemented:

$$0 \leq A \leq 15; \quad 4 \leq B \leq 8191$$

and therefore the range of the overall feedback divider ratio results in:

$$64 \leq N \leq 131071.$$

The user does not need to care about the A- and B-counter settings. It is only necessary to know the overall feedback divider ratio N to program the register settings.

3.1.4 Phase-Frequency Detector

The phase-frequency detector creates an error voltage proportional to the phase difference between the reference signal f_R and f_N . The implementation of the phase detector is a phase-frequency type. That circuitry is very useful because it decreases the acquisition time significantly. The gain of the phase detector can be expressed as:

$$K_{PD} = \frac{I_{CP}}{2\pi}$$

where I_{CP} is the charge pump current which is set via register CPCUR. In the TH71221 design the VCO frequency control characteristic is with negative polarity. This means the VCO frequency increases if the loop filter output voltage decreases and vice versa. In case an external varactor diode is added to the VCO tank, the tuning characteristic can be changed between positive and negative depending on the particular varactor diode circuitry. Therefore the PDFPOL register can be used to define the phase detector polarity.

3.1.5 Lock Detector

In Programmable User Mode a lock-detect signal LD is available at pin FS1/LD (pin 19). The lock detection circuitry uses Up and Down signals from the phase detector to check them for phase coherency. Figure 4 shows an overview of the lock signal generation. The locked state and the unlock condition will be decided on the register settings of LDTM and ERTM respectively. In the start-up phase of the PLL, Up and Down signals are quite unbalanced and counter CNT_LD receives no clock signal. When the loop approaches steady state, the signals Up and Down begin to overlap and CNT_LD counts down. Herein register LDTM sets the number of counts which are necessary to set the lock detection signal LD. If an unlock condition occurs, the counter CNT_LD will be reloaded and therefore its CARRY falls back.

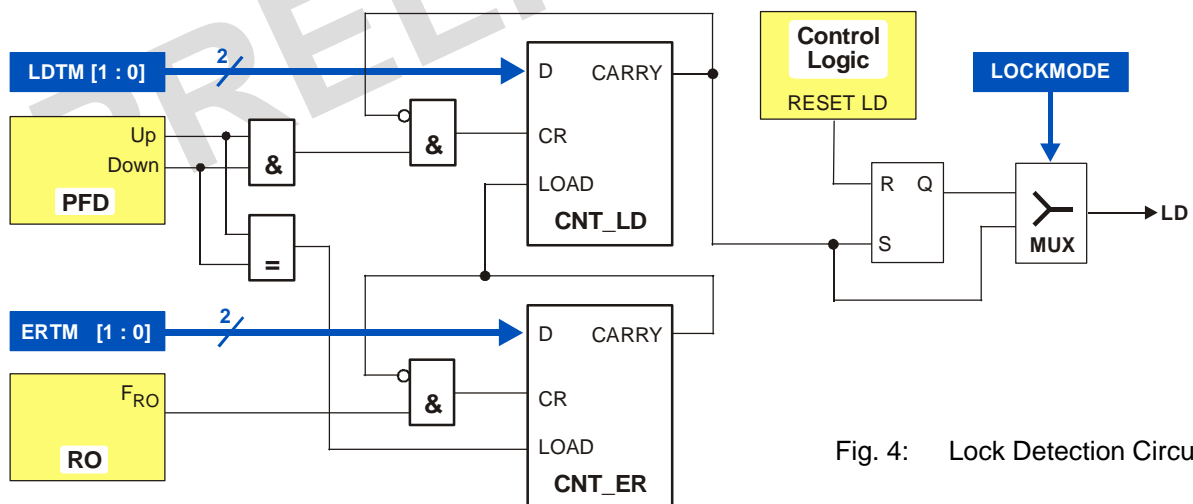


Fig. 4: Lock Detection Circuit

The CNT_ER supervises the unlock condition. If Up and Down are consecutive, the counter CNT_ER will be reloaded permanently and its CARRY will not be set, otherwise the counter level of CNT_ER will be reduced by the reference oscillator clock ($1/f_{RO}$). The register ERTM decides on the maximum number of clocks during Up and Down signals can be non-consecutive without losing the locked state.

The transceiver offers two ways of analyzing the locked state. If the register LOCKMODE is set to '0', only one occurrence of the locked state condition is needed to remain LD = 1 during the whole active mode, otherwise the state of the PLL will be observed permanently.

3.1.6 Voltage Controlled Oscillator with external Loop Filter

The transceiver provides a LC-based voltage-controlled oscillator with an external inductance element connected between VCC and pin TNK_LO. An internal varactor diode in series with a fixed capacitor forms the variable part of the oscillator tank. The oscillation frequency is adjusted by the DC-voltage at pin LF. The tuning sensitivity of the VCO is approximately 20MHz/V for 433MHz operations and 40MHz/V at 868MHz. Since the internal varactor is connected to VCC, a lower voltage on pin LF causes the capacitance to decrease and the VCO frequency to increase. For this reason the phase detector polarity should be negative (PFDPOL = 0). If the operation frequency is below 300MHz, an external varactor diode between pin TNK_LO and VCC_PLL is necessary. The corresponding application schematic is shown in section 8. The VCO current VCOCUR can be adjusted via serial control interface in order to ensure stable oscillations over the whole frequency range. For lowest LO emission in receive mode, VCOCUR should be set to the lowest value.

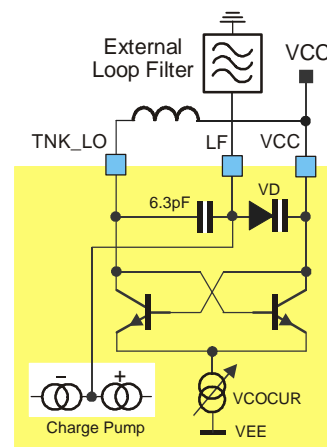


Fig. 5: VCO schematic

3.1.7 Loop Filter

Since the loop filter has a strong impact on the function of the PLL, it must be chosen carefully. For FSK operation the bandwidth of the loop filter must be selected wide enough for a fast relock of the PLL during crystal pulling. The bandwidth must of course also be larger than the data rate. In case of ASK or OOK the bandwidth should be extended even further to allow the PLL to cancel out VCO perturbations that might be caused by the PA on/off keying. The suggested filter topology is shown in Fig. 6. The dimensions of the loop filter elements can be derived using well known formulas in application notes and other reference literature.

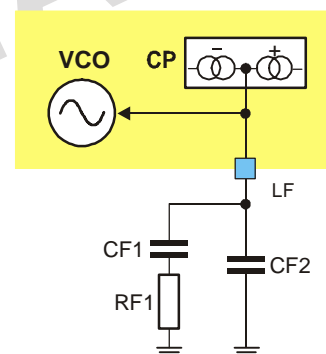


Fig. 6: 2nd order Loop filter

3.2 Receiver Part

The RF front-end of the receiver part is a super-heterodyne configuration that converts the input radio-frequency (RF) signal into an intermediate frequency (IF) signal. The most commonly used IF is 10.7 MHz, but IFs in the range of 450 kHz to 25 MHz can also be used. According to the block diagram, the front-end consists of a LNA, a Mixer and an IF limiting amplifier with received signal strength indicator (RSSI). The local oscillator (LO) signal for the mixer is generated by the PLL frequency synthesizer.

As the receiver constitutes a superhet architecture, there is no inherent suppression of the image frequency. It depends on the particular application and the system's environmental conditions whether an RF front-end filter should be added or not. If image rejection and/or good blocking immunity are relevant system parameters, a band-pass filter must be placed either in front or after the LNA. This filter can be a SAW (surface acoustic wave) or LC-based filter (e.g. helix type).

3.2.1 LNA

The LNA is based on a cascode topology for low-noise, high gain and good reverse isolation. The open collector output has to be connected two an external resonance circuit which is tuned to the receive frequency. The gain of the LNA can be changed in order to achieve a high dynamic range. There are two possibilities for the gain setting which can be selected by the register bit LNACTRL. External control can be done via the pin GAIN_LNA, internal control is given by the register bit LNAGAIN. In case of external gain control, a hysteresis of about 340 mV can be chosen via the register bit LNAHYST. This configuration is useful if an automatic gain control loop via the RSSI signal is established. In transmit mode the LNA-input is shorted to protect the amplifier from saturation and damaging.

3.2.2 Mixer

The mixer is a double-balanced mixer which down converts the receive frequency to the IF frequency. The preferred LO injection type is low side. The output of the mixer is about 330Ohm in order to match the IF channel selection filter.

3.2.3 IF Amplifier

After passing the channel select filter which sets the IF bandwidth the signal is limited by means of an high gain limiting amplifier. The small signal gain is about 80 dB. The RSSI signal is generated within the IF amplifier. The output of the RSSI signal is available at pin RSSI. The voltage at this pin is proportional to the input power of the receiver in dBm. Using this RSSI output signal the signal strength of different transmitters can be distinguished.

3.2.4 ASK Demodulator

The receive part of the TH71221 allows for two ASK demodulation configurations:

- standard ASK demodulation or
- ASK demodulation with peak detector.

The default setting is standard ASK demodulation. In this mode SW1 and SW2 are closed and the RSSI output signal directly feeds the data slicer setup by means of OA1. The data slicer time constant equals to

$$T = 200k\Omega \cdot C3,$$

with C3 external to pin INT1. This time constant should be larger than the longest possible bit duration time of the data. This is required to properly extract the ASK data's DC level. The purpose of the DC (or mean) level at the negative input of OA1 is to set an adaptive comparator threshold to perform the ASK detection.

Alternatively a peak detector can be used to define the ASK detection threshold. In this configuration the peak detector PKDET is enabled, SW1 is closed and SW2 is open, and the peak detector output is multiplexed to pin INT2/PDO. This way the peak detector can feed the data slicer, again constituted by OA1 and a few external R and C components. The peak detection mode is selectable in programmable user mode.

3.2.5 FSK Demodulator

The implemented FSK demodulator is based on the phase-coincidence principle. A discriminator tank, which can either consist of a ceramic discriminator or an LC tank, is connected to pin IN_DEM. If FSK mode is selected SW1 is open, SW2 is closed and the output of OA2 is multiplexed to pin INT2/PDO.

An on-chip AFC circuit tolerates input frequency variations. The input frequency acceptance range is proportional to the FSK or FM deviation. It can be adjusted by the discriminator tank. The AFC feature is enabled by default and can be deactivated in programmable mode.

3.3 Transmitter Part

The output of the PLL frequency synthesizer feeds a power amplifier (PA) in order to setup a complete RF transmitter. The VCO frequency is identical to the carrier frequency.

3.3.1 Power Amplifier

The power amplifier (PA) has been designed to deliver about 10 dBm in the specified frequency bands. Its pin OUT_PA is an open collector output. The larger the output voltage swing can be made the better the power efficiency will be. The PA must be matched to deliver the best efficiency in terms of output power and current consumption.

The collector must be biased to the positive supply. This is done by means of an inductor parallel tuned with a capacitor. Or it is made large enough in order not to affect the output matching network. S-parameters of pin OUT_PA are not useful because the output is very high resistive with a small portion of parallel capacitance. Since the open-collector output transistor can be considered as a current source, the only parameters needed to design the output matching network is the output capacitance, the supply voltage V_{CC} , the transistor's saturation voltage and the power delivered to the load P_O .

In order to avoid saturation of the output stage, a saturation voltage $V_{CE_{SAT}}$ of about 0.7 V should be considered. The real part of the load impedance can then be calculated using

$$R_L = \frac{(V_{CC} - V_{CE_{SAT}})^2}{2 \cdot P_O}$$

The output capacitance is typically 3 pF.

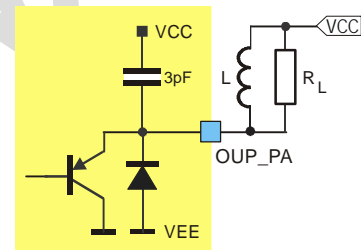


Fig. 7: OUT_PA schematic

3.3.2 Output Power Adjustment

The output power is adjusted via the external resistor RPS as shown in Figure 8. There are furthermore four predefined power settings in programmable user mode which can be set in the register TXPOWER. By default the highest power setting P_{TX_11} is active.

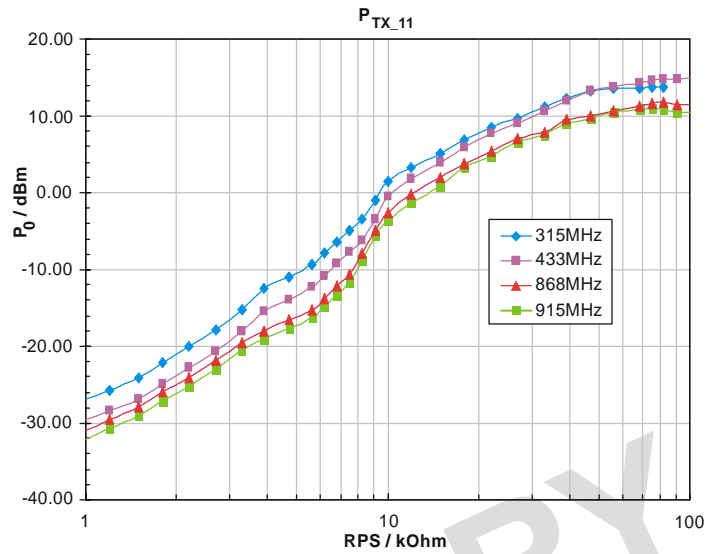


Fig. 8: Output power vs. RPS

3.3.3 Modulation Schemes

The RF carrier generated by the PLL frequency synthesizer can be ASK or FSK modulated. Depending on the selected user mode, the modulation type can be either selected by the ASK/FSK pin or via the serial control interface. Data is applied to pin IN_DTA.

3.3.4 ASK Modulation

IN_DTA	Description
0	Power amplifier is turned off
1	Power amplifier is turned on (according to the selected output power)

The transceiver is ASK-modulated by turning on and off the power amplifier. Please refer also to para. 1.3 of this document.

3.3.5 FSK Modulation

- FSK modulation via crystal pulling

FSK modulation can be achieved by pulling the crystal oscillator frequency. A CMOS-compatible data stream applied at the pin IN_DTA digitally modulates the XOSC via an integrated NMOS switch. Two external pulling capacitors CX1 and CX2 allow the FSK deviation Δf and center frequency f_c to be adjusted independently. At IN_DTA = Low CX2 is connected in parallel to CX1 leading to the low-frequency component of the FSK spectrum (f_{min}); while at IN_DTA = High CX2 is deactivated and the XOSC is set to its high frequency, leading to f_{max} .

IN_DTA	Description
0	$f_{min} = f_c - \Delta f$ (FSK switch is closed)
1	$f_{max} = f_c + \Delta f$ (FSK switch is open)

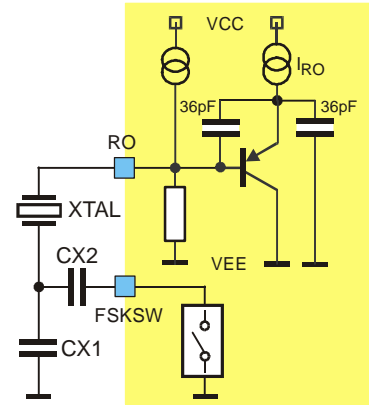


Fig. 9: Crystal Pulling Circuit

An external reference signal can be directly AC-coupled to the reference oscillator input pin RO. Then the transceiver is used without a XTAL. Now the reference signal sets the carrier frequency and has to contain the FSK (or FM) modulation

- FSK modulation via direct VCO modulation

Alternatively FSK or FM can be achieved by injecting the modulating signal into the loop filter to directly control the VCO frequency. Fig. 9 shows a circuit proposal for direct VCO modulation. This circuit is recommended for data rates in excess of about 20 kbps NRZ. An external VCO tuning varactor should be added for narrow-band applications, for example at channel spacings of 25 kHz. For details please refer to the application notes "TH7122 and TH71221 High Speed Data Communication" and "TH7122 and TH71221 Used In Narrow Band FSK Applications"

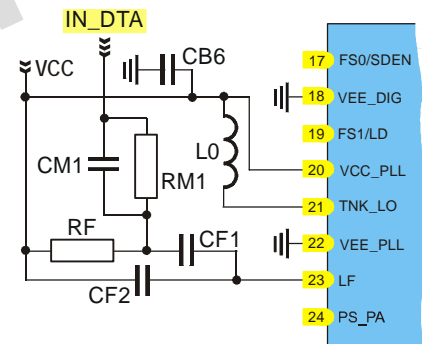


Fig. 10: Circuit schematic for direct VCO modulation

3.3.6 Crystal Tuning

A crystal is tuned by the manufacturer to the requested oscillation frequency f_0 for a certain load capacitance CL within the specified calibration tolerance. The only way to tune this oscillation frequency is to vary the effective load capacitance CL_{eff} seen by the crystal.

Figure 8 shows the oscillation frequency of a crystal in dependency on the effective load capacitance. This capacitance changes in accordance with the logic level of IN_DTA around the specified load capacitance. The figure illustrates the relationship between the external pulling capacitors and the frequency deviation.

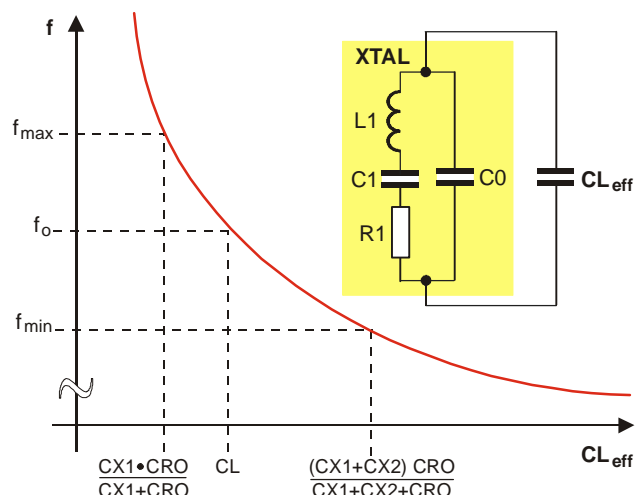


Fig. 11: Crystal Tuning Characteristic

4 Description of User Modes

4.1 Stand-alone User Mode Operation

After power up the transceiver is set to stand-alone user mode. In this mode, pins FS0/SDEN and FS1/LD must be connected to V_{EE} or V_{CC} to set the desired frequency of operation. The logic levels at pins FS0/SDEN and FS1/LD must not be changed after power up in order to remain in stand-alone user mode. The default settings of the control word bits in stand-alone user mode are described in the frequency selection table.

4.1.1 Frequency Selection

Channel frequency	433.92 MHz	868.3 MHz	315 MHz	915 MHz
FS0/SDEN	1	0	1	0
FS1/LD	0	0	1	1
Reference oscillator frequency				
	7.1505 MHz			
R counter ratio in RX mode	32	16	18	32
PFD frequency in RX mode	223.45 kHz	446.91 kHz	397.25 kHz	223.45 kHz
N/A counter ratio in RX mode	1894	1919	766	4047
VCO frequency in RX mode	423.22 MHz	857.60 MHz	304.30 MHz	904.30 MHz
RX frequency	433.92 MHz	868.30 MHz	315.00 MHz	915.00 MHz
R counter ratio in TX mode	32	16	18	32
PFD frequency in TX mode	223.45 kHz	446.91 kHz	397.25 kHz	223.45 kHz
N/A counter ratio in TX mode	1942	1943	793	4095
VCO frequency in TX mode	433.92 MHz	868.30 MHz	315.00 MHz	915.00 MHz
TX frequency	433.92 MHz	868.30 MHz	315.00 MHz	915.00 MHz
IF in RX mode	10.7 MHz	10.7 MHz	10.7 MHz	10.7 MHz

In the stand-alone user mode, the transceiver can be set to Standby, Receive, Transmit or Idle (only PLL synthesizer active) mode via control pins RE/SCLK and TE/SDTA.

Operation mode	Standby	Receive	Transmit	Idle
RE/SCLK	0	1	0	1
TE/SDTA	0	0	1	1

Note: Pins with internal pull-down

In this mode, the modulation type selection can be done via pin ASK/FSK

Modulation type	ASK	FSK
ASK / FSK	0	1

4.2 Programmable User Mode Operation

The transceiver can also be used in the programmable user mode. After power-up the first logic change at pin FS0/SDEN enters into this mode. Now the full functionality is accessible via the Serial Control Interface (SCI).

4.2.1 Serial Control Interface Description

A 3-wire (SCLK, SDTA, SDEN) Serial Control Interface (SCI) is used to program the transceiver in programmable user mode. At each rising edge of the SCLK signal, the logic value on the SDTA pin is written into a 24-bit shift register. The data stored in the shift register are loaded into one of the 4 appropriate latches on the rising edge of SDEN. The control words are 24 bits lengths: 2 address bits and 22 data bits. The first two bits (bit 23 and 22) are latch address bits. As additional leading bits are ignored, only the least significant 24 bits are serial-clocked into the shift register. The first incoming bit is the most significant bit (MSB). To program the transceiver in multi-channel application, four 24-bit words may be sent: A-word, B-word, C-word and D-word. If individual bits within a word have to be changed, then it is sufficient to program only the appropriate 24-bit word. The serial data input timing and the structure of the control words are illustrated in Fig. 12 and 13.

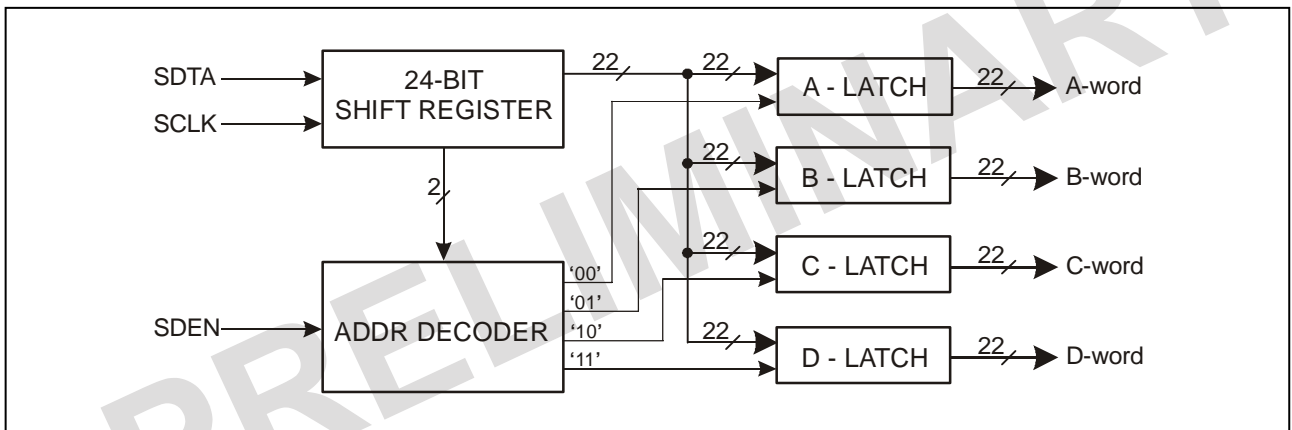


Fig. 12: SCI Block Diagram

Due to the static CMOS design, the SCI consumes virtually no current and it can be programmed in active as well as in standby mode.

If the transceiver is set from standby mode to any of the active modes (idle, receive, transmit), the SCI settings remain the same as previously set in one of the active modes, unless new settings are done on the SCI while entering into an active mode.

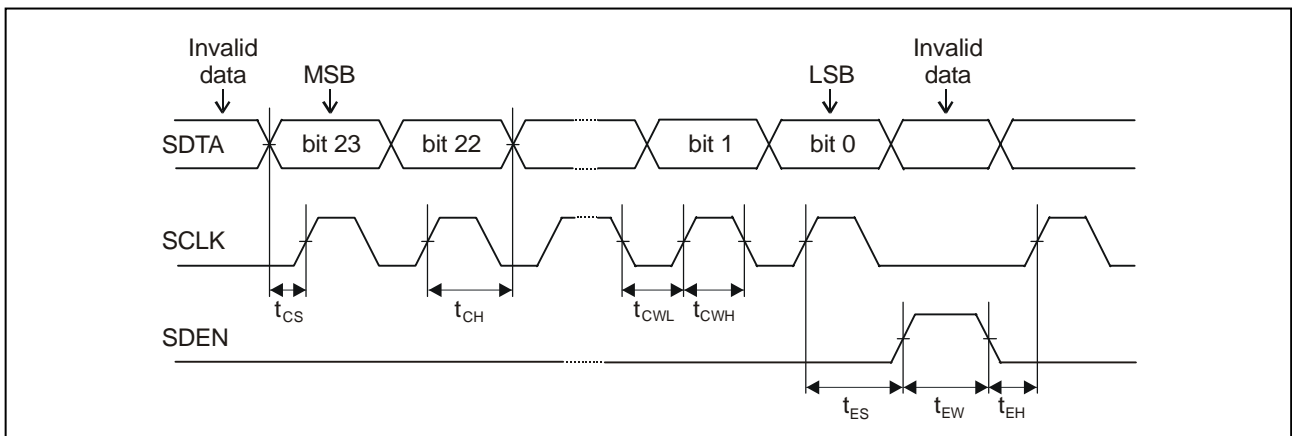


Fig. 13: Serial Data Input Timing

5 Register Description

As shown in the previous section there are four control words which stipulates the operation of the whole chip. In Stand-alone User Mode SUM the intrinsic default values with respect to the applied levels at pins FS0 and FS1 lay down the configuration of the transceiver. In Programmable User Mode PUM the register settings can be changed via 3-wire interface SCI. The following table depicts an overview of the register configuration of the TH71221.

5.1 Register Overview

WORD		DATA																							
MSB																				LSB					
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bit No.	
0	0	0	0	0	0	0	1	1	1	1	1	0	0	Depends on FS0/FS1 voltage level after power up									default		
A		IDLE	DATAPOL	MODSEL	CPCUR	LOCKMODE	PACTRL	TXPOWER [1:0]	Set to 1	LNAGAIN	OPMODE [1:0]	RR [9:0]													
		23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5		4	3	2	1
0	1	0	1	1	1	0	0	1	1	1	0	1	0	Depends on FS0/FS1 voltage level after power up									default		
B		PKDET	Set to 1	DELPLL	LNAHYST	AFC	OA2	ROMAX [2:0]	ROMIN [2:0]			RT [9:0]													
		23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5		4	3	2	1
1	0	0	0	Depends on FS0/FS1 voltage level after power up																		default			
C		LNACTRL	PFDPOL	VCOCUR [1:0]	BAND	NR [16:0]																			
		23	22	21	20	19	18	17	16	15	14	13	12	11		10	9	8	7	6	5	4	3	2	1
1	1	0	0	1	0	0	Depends on FS0/FS1 voltage level after power up																		default
D		MODCTRL	LDTM [1:0]	ERTM [1:0]	NT [16:0]																				
		23	22	21	20	19	18	17	16	15	14	13	12		11	10	9	8	7	6	5	4	3	2	1

The default settings which vary with the desired working frequency depend on the voltage levels at the frequency selection pins FS0 and FS1. The next table shows the default register settings of different frequency selections. It should be noted that the channel frequency listed below will be achieved with a crystal frequency of 7.1505 MHz.

5.1.1 Register Default Settings vs FS0, FS1

FS1	FS0	Channel frequency	BAND	VCOCUR [1:0]	RR [9:0]	NR [16:0]	RT [9:0]	NT [16:0]
0	0	868.30 MHz	1	3	16	1919	16	1943
0	1	433.92 MHz	0	1	32	1894	32	1942
1	0	915.00 MHz	1	3	32	4047	32	4095
1	1	315.00 MHz	0	0	18	766	18	793

A detailed description of the registers function and their configuration can be found in the following sections.

PRELIMINARY

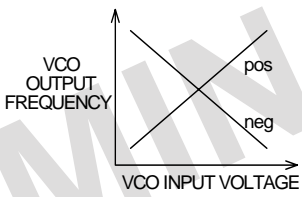
5.1.2 A – word

Name	Bits	Description	
RR	[9:0]	Reference divider ratio in RX operation mode	
		4d .. 1023d	
OPMODE	[11:10]	Operation mode	
		00	Standby mode #default
		01	Receive mode
		10	Transmit mode
		11	Idle mode
LNAGAIN	[12]	LNA gain	
		0	low LNA gain #default
		1	high LNA gain
		This selection is valid if bit LNACTR (bit 21 in C-word) is set to internal LNA gain control.	
not used	[13]	set to '1' for correct function	
TXPOWER	[15:14]	Output power attenuation	
		00	P _{TX_00}
		01	P _{TX_01}
		10	P _{TX_10}
		11	P _{TX_11} #default
		The power selection resistor R _{PS} connected between pin PS_PA and ground selects the output power P ₀ .	
PACTRL	[16]	Set the PA-on condition	
		0	PA is switched on if the PLL locks #default
LOCKMODE	[17]	Set the PLL locked state observation mode	
		0	before lock only #default
		Locked state condition will be ascertained only one time afterwards the LD signal remains in high state.	
		1	before and after lock
		locked state will be observed permanently	
CPCUR	[18]	Charge Pump output current	
		0	± 260 µA #default
		1	±1300 µA
MODSEL	[19]	Modulation mode	
		0	ASK #default
		1	FSK
		This selection is valid if bit MODCTRL (bit 21 in D-word) is set to internal modulation control.	
DTAPOL	[20]	Input data polarity	
		0	normal #default
		'0' for space at ASK or f _{min} at FSK, '1' for mark at ASK or f _{max} at FSK	
		1	inverse
		'1' for space at ASK or f _{min} at FSK, '0' for mark at ASK or f _{max} at FSK	
IDLESEL	[21]	Active blocks in IDLE mode	
		0	only RO is active #default
		1	whole PLL is active

5.1.3 B - word

Name	Bits	Description	
RT	[9:0]	Reference divider ratio in TX operation mode	
		4d .. 1023d	
ROMIN	[12:10]	Set the desired steady state current of the reference oscillator	
		000	0 μ A
		001	75 μ A
		010	150 μ A
		011	225 μ A
		100	300 μ A
		101	375 μ A
		110	450 μ A
		111	525 μ A
		#default	The control circuitry regulates the current of the oscillator core between the values ROMAX and ROMIN. As the regulation input signal the amplitude on pin RO is used. If the ROMIN value is sufficient to achieve an amplitude of about 400mV on pin RO the current of the reference oscillator core will be set to ROMIN. Otherwise the current will be permanently regulated between ROMAX and ROMIN. If ROMIN and ROMAX are equal no regulation of the oscillator current occurs. Please also note the block description of the reference oscillator in para. 3.1.1
ROMAX	[15:13]	Set the start-up current of the reference oscillator	
		000	0 μ A
		001	75 μ A
		010	150 μ A
		011	225 μ A
		100	300 μ A
		101	375 μ A
		110	450 μ A
		111	525 μ A
		#default	Set the start-up current of the reference oscillator core. Please also note the description of the ROMIN register and the block description of the reference oscillator which can be seen above.
OA2	[16]	OA2 operation	
		0	disabled
		1	enabled
		#default	
OA2 can be enabled in FSK receive mode. OA2 is disabled in ASK mode receive.			
AFC	[17]	Internal AFC feature	
		0	disabled
		1	enabled
		#default	
LNAHYST	[18]	Hysteresis on pin GAIN_LNA	
		0	disabled
		1	enabled - typical 340 mV ($V_{0 \rightarrow 1} = 1.56V, V_{1 \rightarrow 0} = 1.22V$)
		#default	
DELPLL	[19]	Delayed start of the PLL	
		0	undelayed start
		PLL starts at the reference oscillator start-up	
		1	starts after 8 valid RO-cycles
		#default	
PLL starts after 8 valid RO-cycles before entering an active mode to ensure reliable oscillation of the reference oscillator.			
not used	[20]	set to '1' for correct function	
PKDET	[21]	RSSI Peak Detector	
		0	disabled
		#default	
The RSSI output signal directly feeds the data slicer setup by means of OA1.			
		1	enabled
In ASK receive mode the RSSI Peak Detector output is multiplexed to pin INT2/PDO.			

5.1.4 C - word

Name	Bits	Description
NR	[16:0]	Feedback divider ratio in RX operation mode
		64d .. 131071d
BAND	[17]	Set the desired frequency range
		0 recommended at $f_{RF} < 500$ MHz
		1 recommended at $f_{RF} > 500$ MHz
Some tail current sources are linked to this bit in order to save current for low frequency operations.		
VCOCUR	[19:18]	VCO active current
		00 low current (300 μ A)
		01 standard current (500 μ A)
		10 high1 current (700 μ A)
		11 high2 current (900 μ A)
PFDPOL	[20]	Phase Detector polarity
		0 negative #default
		1 positive
		
LNACTRL	[21]	LNA gain control mode
		0 external LNA gain control #default
		LNA gain will be set via pin GAIN_LNA.
1 internal LNA gain control		
LNA gain will be set via bit LNAGAIN (bit 12 in A-word).		

5.1.5 D - word

Name	Bits	Description		
NT	[16:0]	Feedback divider ratio in TX operation mode 64d .. 131071d		
ERTM	[18:17]	Set the unlock condition of the PLL		
		00	2 clocks	#default
		01	4 clocks	
		10	8 clocks	
		11	16 clocks	
LDTM	[20:19]	Set the lock condition of the PLL		
		00	4 clocks	#default
		01	16 clocks	
		10	64 clocks	
		11	256 clocks	
MODCTRL	[21]	Set mode of modulation control:		
		0	external modulation control	#default
			modulation will be set via pin ASK/FSK	
		1	internal modulation control	
		modulation will be set via bit MODSEL (bit 19 in A-word)		

PRELIMINARY

6 Technical Data

6.1 Absolute Maximum Ratings

Parameter	Symbol	Condition / Note	Min	Max	Unit
Supply voltage	V_{CC}		0	7.0	V
Input voltage	V_{IN}		- 0.3	$V_{CC}+0.3$	V
Input RF level	P_{iRF}	@ LNA input		10	dBm
Storage temperature	T_{STG}		-40	+125	°C
Junction temperature	T_J			+150	°C
Power dissipation	P_{diss}			0.25	W
Thermal Resistance	R_{thJA}			60	K/W
Electrostatic discharge	V_{ESD1}	human body model, 1)	-1.0	+1.0	kV
Electrostatic discharge	V_{ESD2}	human body model, 2)	TBD	TBD	kV

1) pins IN_DTA, ASK/FSK, RE/SCLK; TE/SDTA, FS0/SDEN, FS1/LD

2) all pins, except IN_DTA, ASK/FSK, RE/SCLK; TE/SDTA, FS0/SDEN, FS1/LD

6.2 Normal Operating Conditions

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage	V_{CC}		2.2	5.5	V
Operating temperature	T_A		-40	+85	°C
Input low voltage (CMOS)	V_{IL}	IN_DTA, RE/SCLK, TE/SDTA, ASK/FSK, FS0/SDEN, FS1/LD pins		$0.3 \cdot V_{CC}$	V
Input high voltage (CMOS)	V_{IH}	IN_DTA, RE/SCLK, TE/SDTA, ASK/FSK, FS0/SDEN, FS1/LD pins	$0.7 \cdot V_{CC}$		V
Transmit frequency range	f_{TX}		300	930	MHz
Receive frequency range	f_{RX}		300	930	MHz
VCO frequency	f_{VCO}	Set by tank configuration	300	930	MHz
IF range	f_{IF}	$f_{RX} - f_{VCO}$	0.4	22	MHz
RO frequency	f_{RO}	Set by crystal	3	12	MHz
PFD working frequency	f_{PFD}	Set by crystal and R-counter	0.01	1	MHz
Frequency deviation	Δf	at FM or FSK	± 2.5	± 80	kHz
FSK data rate	R_{FSK}	w/ crystal puling, NRZ		20	kbps
		w/ direct VCO mod., NRZ		115	kbps
ASK data rate	R_{ASK}	NRZ		40	kbps
FM bandwidth	f_m			10	kHz
VCO gain	K_{VCO}	$f_{RF} = 433.92\text{MHz}$	14	23	MHz/V
		$f_{RF} = 868.3\text{MHz}$	28	55	

6.3 DC Characteristics

all parameters under normal operating conditions, unless otherwise stated;
typical values at $T_A = 23\text{ °C}$ and $V_{CC} = 3\text{ V}$

Parameter	Symbol	Condition	Min	Typ	Max	Unit		
Standby current	I_{SBY}	mode = standby		50	100	nA		
	Band bit							
Idle current		I_{IDLE}	mode = idle, IDLESEL = 0		0.3		mA	
				0 (< 500 MHz)		3.5		mA
				1 (> 500 MHz)		6.3		mA
Receive supply current - ASK	0 (< 500 MHz)	I_{RXL_ASK}	mode = receive, ASK LNA @ low gain		6.1		mA	
				1 (> 500 MHz)		8.9		mA
	0 (< 500 MHz)	I_{RXH_ASK}	mode = receive, ASK LNA @ high gain		7.4		mA	
				1 (> 500 MHz)		10.2		mA
Receive supply current - FSK	0 (< 500 MHz)	I_{RXL_FSK}	mode = receive, FSK LNA @ low gain		6.7		mA	
				1 (> 500 MHz)		9.5		mA
	0 (< 500 MHz)	I_{RXH_FSK}	mode = receive, FSK LNA @ high gain		8.0		mA	
				1 (> 500 MHz)		10.8		mA
Transmit supply current @ P_{TX_00}	0 (< 500 MHz)	I_{TX_00}	Mode = transmit, RPS = see para. 7.3 TXPOWER = 00		11.5		mA	
	1 (> 500 MHz)				15.5		mA	
Transmit supply current @ P_{TX_01}	0 (< 500 MHz)	I_{TX_01}	Mode = transmit, RPS = see para. 7.3 TXPOWER = 01		12.2		mA	
	1 (> 500 MHz)				16.4		mA	
Transmit supply current @ P_{TX_10}	0 (< 500 MHz)	I_{TX_10}	Mode = transmit, RPS = see para. 7.3 TXPOWER = 10		14		mA	
	1 (> 500 MHz)				17.5		mA	
Transmit supply current @ P_{TX_11}	0 (< 500 MHz)	I_{TX_11}	Mode = transmit, RPS = see para. 7.3 TXPOWER = 11		20		mA	
	1 (> 500 MHz)				24		mA	

6.4 PLL Synthesizer Timings

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Channel switching time	wide band	t_{SW_WB}	$B_{PLL} = 20\text{kHz}$, $I_{CP} = 260\mu\text{A}$		200		μs
	narrow band	t_{SW_NB}	$B_{PLL} = 2\text{kHz}$, $I_{CP} = 260\mu\text{A}$		500		μs
TX – RX switching time		t_{TX_RX}	$IF = 10.7\text{MHz}$		1		ms

6.5 AC System Characteristics of the Receiver Part

all parameters under normal operating conditions, unless otherwise stated; all parameters based on test circuits for FSK (Fig. 14 to 15) and ASK (Fig. 16 to 17), respectively;

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Input sensitivity ASK	$f_{RF} = 433.92\text{MHz}$	P_{minL_ASK}	$B_{IF} = 150\text{kHz}$, $f_m = 2\text{kHz}$ $BER \leq 3 \cdot 10^{-3}$ LNA @ low gain		-96		dBm
	$f_{RF} = 868.3\text{MHz}$				-96		
	$f_{RF} = 433.92\text{MHz}$	P_{minH_ASK}	$B_{IF} = 150\text{kHz}$, $f_m = 2\text{kHz}$ $BER \leq 3 \cdot 10^{-3}$ LNA @ high gain		-107		dBm
	$f_{RF} = 868.3\text{MHz}$				-107		
Input sensitivity FSK	$f_{RF} = 433.92\text{MHz}$	P_{minL_FSK}	$B_{IF} = 150\text{kHz}$, $f_m = 2\text{kHz}$ $\Delta f = \pm 50\text{kHz}$ $BER \leq 3 \cdot 10^{-3}$ LNA @ low gain		-87		dBm
	$f_{RF} = 868.3\text{MHz}$				-87		
	$f_{RF} = 433.92\text{MHz}$	P_{minH_FSK}	$B_{IF} = 150\text{kHz}$, $f_m = 2\text{kHz}$ $\Delta f = \pm 50\text{kHz}$ $BER \leq 3 \cdot 10^{-3}$ LNA @ high gain		-105		dBm
	$f_{RF} = 868.3\text{MHz}$				-105		
Maximum input signal ASK	$f_{RF} = 433.92\text{MHz}$	P_{maxL_ASK}	$B_{IF} = 150\text{kHz}$, $f_m = 2\text{kHz}$ $BER \leq 3 \cdot 10^{-3}$ LNA @ low gain		-10		dBm
	$f_{RF} = 868.3\text{MHz}$				-10		
	$f_{RF} = 433.92\text{MHz}$	P_{maxH_ASK}	$B_{IF} = 150\text{kHz}$, $f_m = 2\text{kHz}$ $BER \leq 3 \cdot 10^{-3}$ LNA @ high gain		-20		dBm
	$f_{RF} = 868.3\text{MHz}$				-20		
Maximum input signal FSK	$f_{RF} = 433.92\text{MHz}$	P_{maxL_FSK}	$B_{IF} = 150\text{kHz}$, $f_m = 2\text{kHz}$ $BER \leq 3 \cdot 10^{-3}$ LNA @ low gain		-10		dBm
	$f_{RF} = 868.3\text{MHz}$				-10		
	$f_{RF} = 433.92\text{MHz}$	P_{maxH_FSK}	$B_{IF} = 150\text{kHz}$, $f_m = 2\text{kHz}$ $BER \leq 3 \cdot 10^{-3}$ LNA @ high gain		-20		dBm
	$f_{RF} = 868.3\text{MHz}$				-20		
Start-up time - ASK		t_{on_ASK}	from standby to receive mode		1	1.5	ms
Start-up time - FSK		t_{on_FSK}	from standby to receive mode		1	1.5	ms
Spurious emission		P_{spur_RX}	referred to receiver input		-54		dBm

6.6 AC System Characteristics of the Transmitter Part

all parameters under normal operating conditions, unless otherwise stated;
 typical values at $T_a = 23\text{ °C}$ and $V_{CC} = 3\text{ V}$;
 all parameters based on test circuits for FSK (Fig. 14 to 15), FM and ASK (Fig. 16 to 17), respectively;

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Output power	$f_{RF} = 433.92\text{MHz}$	P_{TX_00}	mode = transmit, RPS = see para. 7.3 TXPOWER = 00		-10		dBm
	$f_{RF} = 868.3\text{MHz}$				-14		
Output power	$f_{RF} = 433.92\text{MHz}$	P_{TX_01}	mode = transmit, RPS = see para. 7.3 TXPOWER = 01		-2		dBm
	$f_{RF} = 868.3\text{MHz}$				-6		
Output power	$f_{RF} = 433.92\text{MHz}$	P_{TX_10}	mode = transmit, RPS = see para. 7.3 TXPOWER = 10		3		dBm
	$f_{RF} = 868.3\text{MHz}$				-1		
Output power	$f_{RF} = 433.92\text{MHz}$	P_{TX_11}	mode = transmit, RPS = see para. 7.3 TXPOWER = 11		10		dBm
	$f_{RF} = 868.3\text{MHz}$				8		
FSK deviation		Δf_{FSK}	depends on C_{x1} , C_{x2} and crystal parameters	± 2.5	± 25	± 80	kHz
FM deviation		Δf_{FM}	adjustable with varactor and V_{FM}		± 6		kHz
Modulation frequency FM		f_{mod}				10	kHz
PLL reference spurious emission		P_{spur_PLL}				-40	dBm
Harmonic emission		P_{harm}				-36	dBm
Start-up time		t_{on_TX}	From standby to transmit mode		1	1.5	ms

6.7 Serial Control Interface

Parameter	Symbol	Condition	Min	Max	Unit
SDTA to SCLK set up time	t_{CS}		150		ns
SCLK to SDTA hold time	t_{CH}		50		ns
SCLK pulse width low	t_{CWL}		100		ns
SCLK pulse width high	t_{CWH}		100		ns
SCLK to SDEN set up time	t_{ES}		100		ns
SDEN pulse width	t_{EW}		100		ns
SDEN to SCLK hold time	t_{EH}		100		ns

6.8 Crystal Parameters

Parameter	Symbol	Condition	Min	Max	Unit
Crystal frequency	$f_{crystal}$	fundamental mode, AT	3	12	MHz
Load capacitance	C_{load}		10	15	pF
Static capacitance	C_0			7	pF
Series resistance	R_1			70	Ω
Spurious response	a_{spur}	only required for FSK		-10	dB

7 Application Circuit Examples

7.1 FSK Application Circuit Programmable User Mode (internal AFC option)

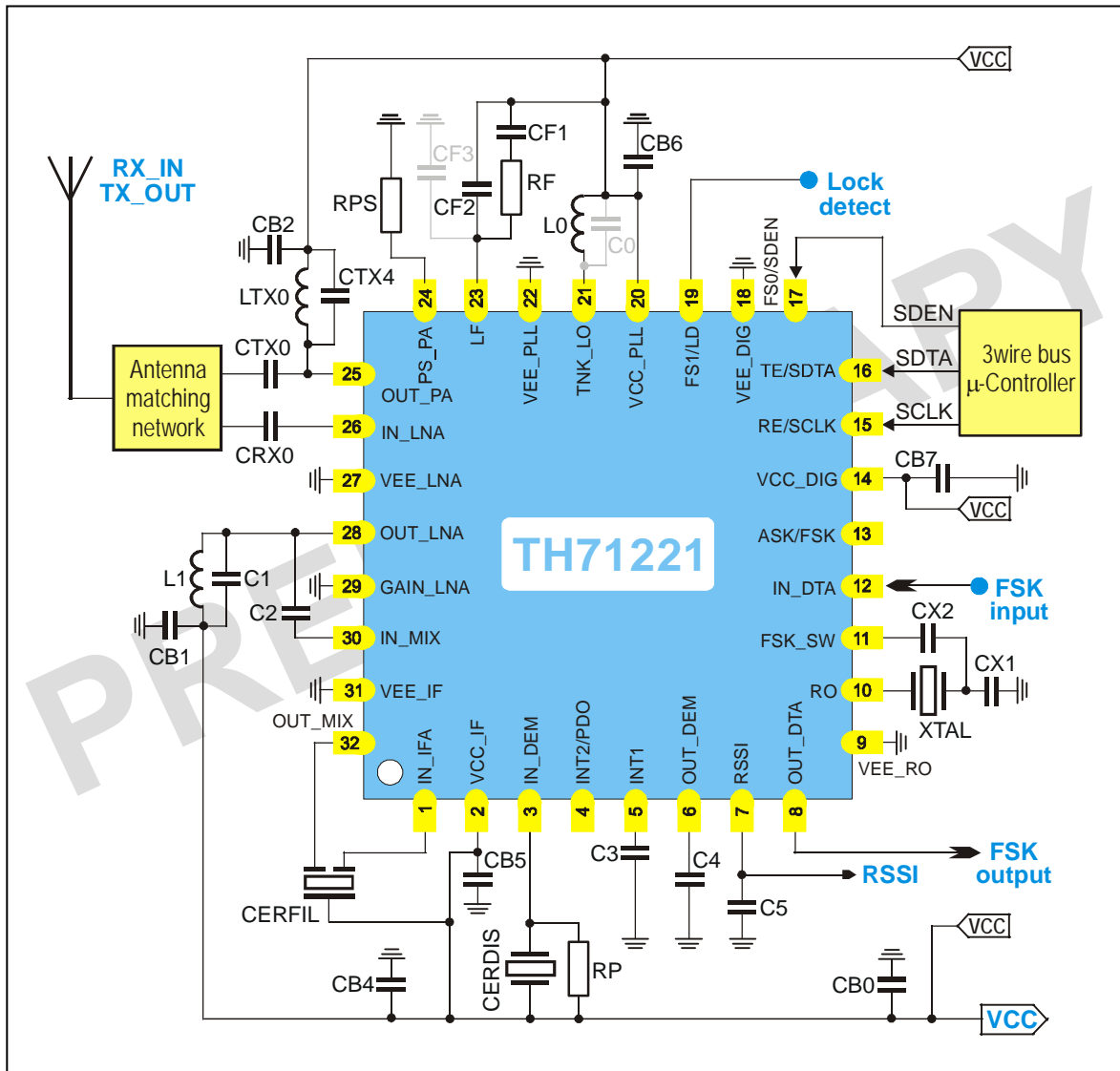


Fig. 14: Test circuit for FSK operation in Programmable User Mode (internal AFC by default)

7.2 FSK Application Circuit Stand-alone User Mode

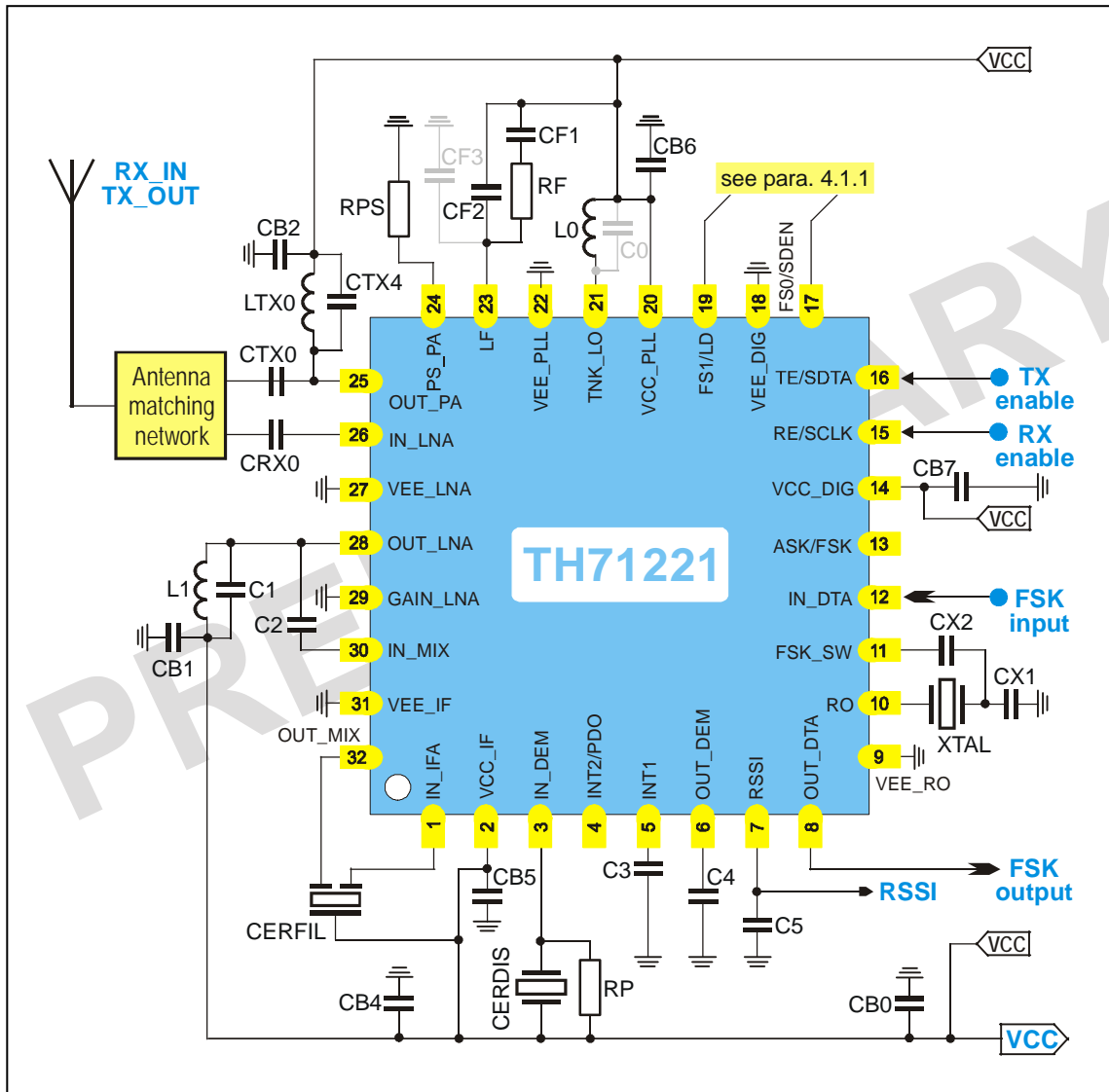


Fig. 15: Test circuit for FSK operation in Stand-alone User Mode

7.3 FSK Test Circuit Component List (Fig. 14 and Fig. 15)

Part	Size	Value @ 315 MHz	Value @ 433.92 MHz	Value @ 868.3 MHz	Value @ 915 MHz	Tol.	Description
C0	0603	0.68 pF	NIP	NIP	NIP	±5%	VCO tank capacitor
C1	0603	5.6 pF	5.6 pF	1.5 pF	NIP	±5%	LNA output tank capacitor
C2	0603	1.5 pF	1.0 pF	1.5 pF	1.5 pF	±5%	MIX input matching capacitor
C3	0603	10 nF	10 nF	10 nF	10 nF	±10%	data slicer capacitor
C4	0603	330 pF	330 pF	330 pF	330 pF	±5%	demodulator output low-pass capacitor, depending on data rate
C5	0603	1.5 nF	1.5 nF	1.5 nF	1.5 nF	±10%	RSSI output low pass capacitor
CB0	1210	10 µF	10 µF	10 µF	10 µF	±20%	de-coupling capacitor
CB1	0603	330 pF	330 pF	330 pF	330 pF	±10%	de-coupling capacitor
CB2	0805	330 pF	330 pF	330 pF	330 pF	±10%	de-coupling capacitor
CB4	0603	10 nF	10 nF	10 nF	10 nF	±10%	de-coupling capacitor
CB5	0603	100 nF	100 nF	100 nF	100 nF	±10%	de-coupling capacitor
CB6	0603	100 pF	100 pF	100 pF	100 pF	±10%	de-coupling capacitor
CB7	0603	100 nF	100 nF	100 nF	100 nF	±10%	de-coupling capacitor
CF1	0603	1 nF	1 nF	1 nF	1 nF	±10%	loop filter capacitor
CF2	0603	220 pF	150 pF	150 pF	150 pF	±5%	loop filter capacitor
CF3	0603	NIP	NIP	3.9 pF	3.9 pF	±5%	loop filter capacitor
CX1	0805	15 pF	15 pF	18 pF	15 pF	±5%	RO capacitor for FSK ($\Delta f = \pm 20$ kHz)
CX2	0805	150 pF	150 pF	27 pF	22 pF	±5%	RO capacitor for FSK ($\Delta f = \pm 20$ kHz)
CRX0	0603	100 pF	100 pF	100 pF	100 pF	±5%	RX coupling capacitor
CTX0	0603	100 pF	100 pF	100 pF	100 pF	±5%	TX coupling capacitor
CTX4	0603	12 pF	6.8 pF	2.7 pF	3.3 pF	±5%	TX impedance matching capacitor
RF	0603	33 kΩ	33 kΩ	33 kΩ	33 kΩ	±5%	loop filter resistor
RP	0603	3.3 KΩ	3.3 KΩ	3.3 KΩ	3.3 KΩ	±5%	CERDIS loading resistor
RPS	0603	18 kΩ	33 kΩ	47 kΩ	47 kΩ	±5%	power-select resistor
L0	0603			5.6 nH	4.7 nH	±5%	VCO tank inductor
	1008	56 nH	33 nH				
L1	0603			3.9 nH	4.7 nH	±5%	LNA output tank inductor
	1008	27 nH	15 nH				
LTX0	0603			3.9 nH	4.7 nH	±5%	TX impedance matching inductor
	1008	15 nH	15 nH				
XTAL	HC49 SMD	7.1505 MHz (or 8.0000MHz) ±20ppm cal., ±20ppm temp.					fundamental-mode crystal, $C_{load} = 10$ pF to 15pF, $C_{0, max} = 7$ pF, $R_{m, max} = 70 \Omega$
CERFIL	SMD type	SFECV10M7JA00 @ $B_{IF2} = 150$ kHz, ±40kHz					ceramic filter from Murata, or equivalent part
CERDIS	SMD type	CDSCB10M7GA136					ceramic Discriminator from Murata, or equivalent part

Note:

- NIP – not in place, may be used optionally
- Antenna matching network according to paragraph 9

**7.4 ASK Application Circuit Programmable User Mode
(normal data slicer option)**

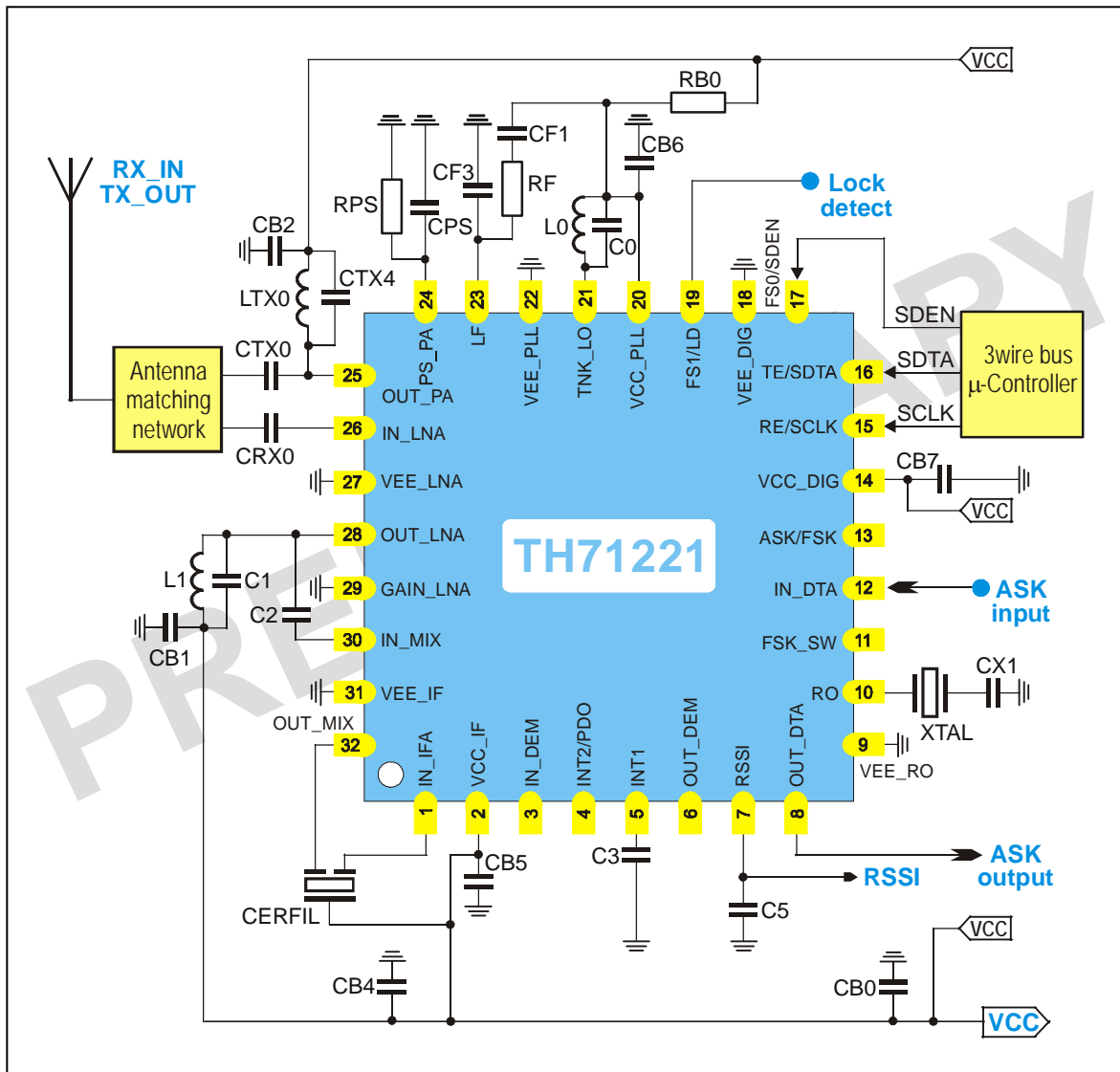


Fig. 16: Test circuit for ASK operation in Programmable User Mode

7.5 ASK Test Circuit Component List (Fig. 16)

Part	Size	Value @ 315 MHz	Value @ 433.92 MHz	Value @ 868.3 MHz	Value @ 915 MHz	Tol.	Description
C0	0603	0.68 pF	2.2 pF	3.9 pF	3.3 pF	±5%	VCO tank capacitor
C1	0603	5.6 pF	5.6 pF	1.5 pF	NIP	±5%	LNA output tank capacitor
C2	0603	1.5 pF	1.0 pF	1.5 pF	1.5 pF	±5%	MIX input matching capacitor
C3	0603	10 nF	10 nF	10 nF	10 nF	±10%	data slicer capacitor
C5	0603	1.5 nF	1.5 nF	1.5 nF	1.5 nF	±10%	RSSI output low pass capacitor
CB0	1210	10 µF	10 µF	10 µF	10 µF	±20%	de-coupling capacitor
CB1	0603	330 pF	330 pF	330 pF	330 pF	±10%	de-coupling capacitor
CB2	0805	330 pF	330 pF	330 pF	330 pF	±10%	de-coupling capacitor
CB5	0603	100 nF	100 nF	100 nF	100 nF	±10%	de-coupling capacitor
CB6	0603	100 pF	100 pF	100 pF	100 pF	±10%	de-coupling capacitor
CB7	0603	100 nF	100 nF	100 nF	100 nF	±10%	de-coupling capacitor
CF1	0603	100 pF	100 pF	100 pF	100 pF	±5%	loop filter capacitor
CF3	0603	39 pF	39 pF	39 pF	39 pF	±5%	loop filter capacitor
CPS	0603	1 nF	1 nF	1 nF	1 nF	±10%	power-select capacitor
CX1	0805	15 pF	15 pF	22 pF	22 pF	±5%	RO capacitor
CRX0	0603	100 pF	100 pF	100 pF	100 pF	±5%	RX coupling capacitor
CTX0	0603	100 pF	100 pF	100 pF	100 pF	±5%	TX coupling capacitor
CTX4	0603	12 pF	6.8 pF	2.7 pF	3.3 pF	±5%	TX impedance matching capacitor
RB0	0603	100 Ω	100 Ω	100 Ω	100 Ω	±5%	protection resistor
RF	0603	33 kΩ	33 kΩ	33 kΩ	33 kΩ	±5%	loop filter resistor
RPS	0603	18 kΩ	33 kΩ	47 kΩ	47 kΩ	±5%	power-select resistor
L0	0603			5.6 nH	4.7 nH	±5%	VCO tank inductor
	1008	56 nH	33 nH				
L1	0603			3.9 nH	4.7 nH	±5%	LNA output tank inductor
	1008	27 nH	15 nH				
LTX0	0603			3.9 nH	4.7 nH	±5%	TX impedance matching inductor
	1008	15 nH	15 nH				
XTAL	HC49 SMD	7.1505 MHz (or 8.0000MHz) ±20ppm cal., ±20ppm temp.					fundamental-mode crystal, C _{load} = 10 pF to 15pF, C _{0,max} = 7 pF, R _{m,max} = 70 Ω
CERFIL	SMD type	SFECV10M7JA00 @ B _{IF2} = 150 kHz, ±40kHz					ceramic filter from Murata, or equivalent part

Note:

- NIP – not in place, may be used optionally
- Antenna matching network according to paragraph 9

**7.6 ASK Application Circuit Programmable User Mode
(internal peak detector option)**

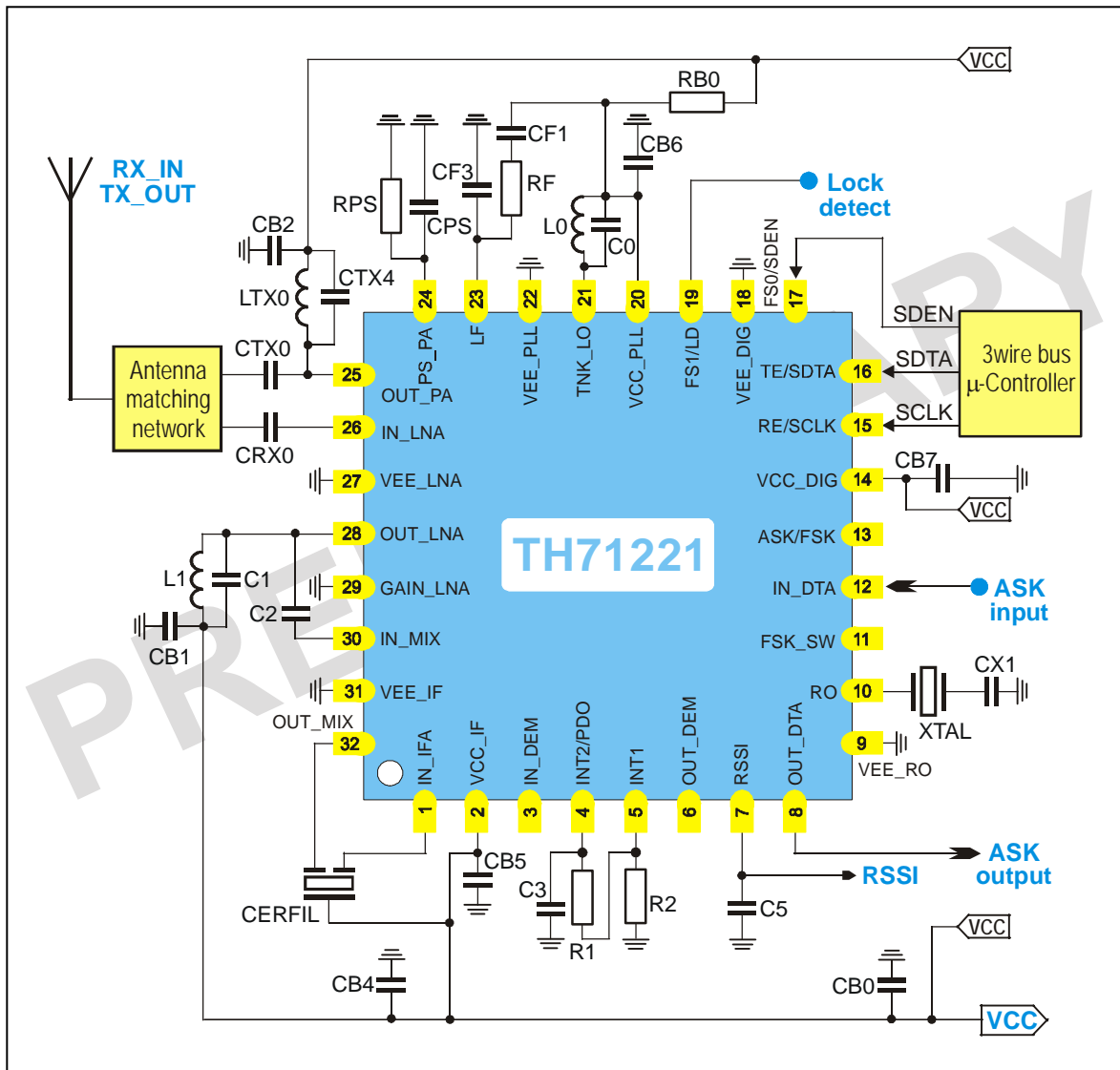


Fig. 17: Test circuit for ASK operation in Programmable User Mode (internal Peak Detector option)

7.7 ASK Test Circuit Component List (Fig. 17)

Part	Size	Value @ 315 MHz	Value @ 433.92 MHz	Value @ 868.3 MHz	Value @ 915 MHz	Tol.	Description
C0	0603	0.68 pF	2.2 pF	3.9 pF	3.3 pF	±5%	VCO tank capacitor
C1	0603	5.6 pF	5.6 pF	1.5 pF	NIP	±5%	LNA output tank capacitor
C2	0603	1.5 pF	1.0 pF	1.5 pF	1.5 pF	±5%	MIX input matching capacitor
C5	0603	1.5 nF	1.5 nF	1.5 nF	1.5 nF	±10%	RSSI output low pass capacitor
C6	0603	100 nF	100 nF	100 nF	100 nF	±10%	PKDET capacitor
CB0	1210	10 µF	10 µF	10 µF	10 µF	±20%	de-coupling capacitor
CB1	0603	330 pF	330 pF	330 pF	330 pF	±10%	de-coupling capacitor
CB2	0805	330 pF	330 pF	330 pF	330 pF	±10%	de-coupling capacitor
CB5	0603	100 nF	100 nF	100 nF	100 nF	±10%	de-coupling capacitor
CB6	0603	100 pF	100 pF	100 pF	100 pF	±10%	de-coupling capacitor
CB7	0603	100 nF	100 nF	100 nF	100 nF	±10%	de-coupling capacitor
CF1	0603	100 pF	100 pF	100 pF	100 pF	±5%	loop filter capacitor
CF3	0603	39 pF	39 pF	39 pF	39 pF	±5%	loop filter capacitor
CPS	0603	1 nF	1 nF	1 nF	1 nF	±10%	power-select capacitor
CX1	0805	15 pF	15 pF	22 pF	22 pF	±5%	RO capacitor
CRX0	0603	100 pF	100 pF	100 pF	100 pF	±5%	RX coupling capacitor
CTX0	0603	100 pF	100 pF	100 pF	100 pF	±5%	TX coupling capacitor
CTX4	0603	12 pF	6.8 pF	2.7 pF	3.3 pF	±5%	TX impedance matching capacitor
R1	0603	100 kΩ	100 kΩ	100 kΩ	100 kΩ	±5%	PKDET resistor
R2	0603	680 kΩ	680 kΩ	680 kΩ	680 kΩ	±5%	PKDET resistor
RB0	0603	100 Ω	100 Ω	100 Ω	100 Ω	±5%	protection resistor
RF	0603	33 kΩ	33 kΩ	33 kΩ	33 kΩ	±5%	loop filter resistor
RPS	0603	18 kΩ	33 kΩ	47 kΩ	47 kΩ	±5%	power-select resistor
L0	0603			5.6 nH	4.7 nH	±5%	VCO tank inductor
	1008	56 nH	33 nH				
L1	0603			3.9 nH	4.7 nH	±5%	LNA output tank inductor
	1008	27 nH	15 nH				
LTX0	0603			3.9 nH	4.7 nH	±5%	TX impedance matching inductor
	1008	15 nH	15 nH				
XTAL	HC49 SMD	7.1505 MHz (or 8.0000MHz) ±20ppm cal., ±20ppm temp.					fundamental-mode crystal, C _{load} = 10 pF to 15pF, C _{0, max} = 7 pF, R _{m, max} = 70 Ω
CERFIL	SMD type	SFECV10M7JA00 @ B _{IF2} = 150 kHz, ±40kHz					ceramic filter from Murata, or equivalent part

Note:

- NIP – not in place, may be used optionally
- Antenna matching network according to paragraph 9

8 Extended Frequency Range

The operating frequency range of 300 MHz to 930 MHz can be covered without the use of an additional VCO varactor diode. A frequency range extension down to 27 MHz can be realized by adding an external varactor diode to the VCO tank.

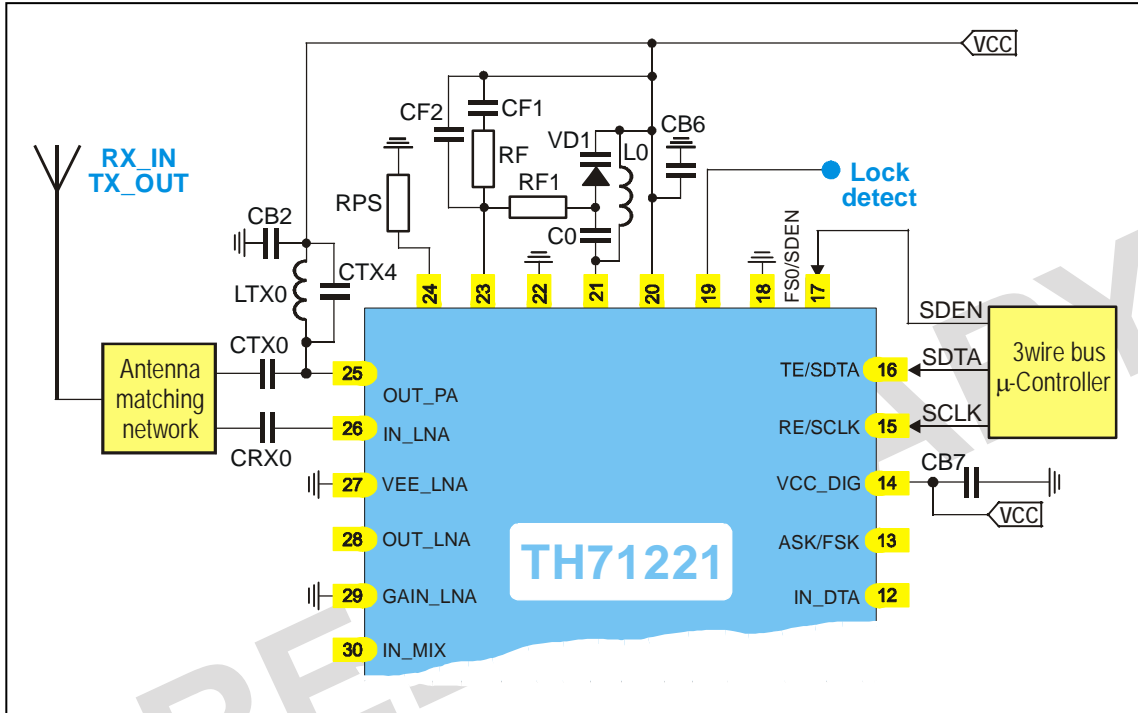


Fig. 18: VCO tank circuit for extended frequency range

8.1 Board Component List (Fig. 18)

Part	Size	Value @ 27 MHz	Value @ 80 MHz	Value @ 170 MHz	Tol.	Description
C0	0805				±5%	VCO tank capacitor
VD1	SOD-323					varactor diode
CF1	0605				±5%	loop filter capacitor
CF2	0605				±5%	loop filter capacitor
RF	0805				±5%	loop filter resistor
RF1	0805				±5%	loop filter resistor
CTX0	0603				±5%	TX coupling capacitor
CRX0	0603				±5%	RX coupling capacitor
L0	0805				±5%	VCO tank inductor
LTX0	0805				±5%	TX impedance matching inductor
CB2	0805	330 pF	330 pF	330 pF	±10%	de-coupling capacitor
CB6	0603	100 pF	100 pF	100 pF	±10%	de-coupling capacitor
CB7	0603	100 nF	100 nF	100 nF	±10%	de-coupling capacitor

Note: All other components are unchanged

9 TX/RX Combining Network

9.1 Board Component List (Fig. 19)

Part	Size	Value @ 315 MHz	Value @ 433.92 MHz	Value @ 868.3 MHz	Value @ 915 MHz
CRX0	0603	100 pF	100 pF	100 pF	100 pF
CTX0	0603	100 pF	100 pF	100 pF	100 pF
CTX1	0805	8.2 pF	5.6 pF	3.9 pF	3.9 pF
CTX2	0805	8.2 pF	4.7 pF	3.9 pF	4.7 pF
CTX4	0603	12 pF	6.8 pF	2.7 pF	3.3 pF
LRX2	0603	100 nH	56 nH	10 nH	6.8 nH
LTX0	0603	15 nH	15 nH	3.9 nH	4.7 nH
LTX1	0603	33 nH	27 nH	8.2 nH	5.6 nH
CB2	0805	330 pF	330 pF	330 pF	330 pF

- No TX/RX switch required
- Direct connection to $\lambda/4$ antenna possible

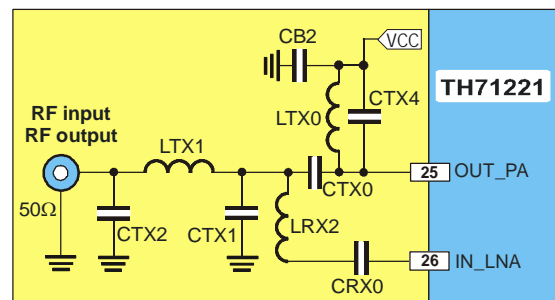


Fig. 19: Combining network schematic

9.2 Typical LNA S-Parameters in Receive Mode

Low Gain Mode

Frequency	Re[S ₁₁]	Im[S ₁₁]	Re[S ₁₂]	Im[S ₁₂]	Re[S ₂₁]	Im[S ₂₁]	Re[S ₂₂]	Im[S ₂₂]
27 MHz	0.9138	-0.0145	6.06E-005	4.27E-004	-0.4172	0.0334	0.9986	-0.0095
40 MHz	0.9139	-0.0229	5.53E-005	6.73E-004	-0.4092	0.0400	0.9984	-0.0136
80 MHz	0.9126	-0.0481	5.36E-005	1.48E-004	-0.3989	0.0581	0.9979	-0.0265
170 MHz	0.9054	-0.1026	7.44E-004	3.25E-003	-0.3828	0.1056	0.9966	-0.0558
315 MHz	0.8836	-0.1814	2.16E-004	6.21E-003	-0.3300	0.1798	0.9926	-0.1033
433 MHz	0.8622	-0.2625	7.81E-004	6.34E-003	-0.3248	0.2168	0.9870	-0.1417
868 MHz	0.7161	-0.4577	2.35E-003	1.09E-003	-0.1265	0.3187	0.9543	-0.2829
915 MHz	0.6975	-0.4753	2.24E-003	1.10E-003	-0.1062	0.3206	0.9494	-0.2980

Note: input and output of the LNA are connected to 50 Ω ports without matching elements

High Gain Mode

Frequency	Re[S ₁₁]	Im[S ₁₁]	Re[S ₁₂]	Im[S ₁₂]	Re[S ₂₁]	Im[S ₂₁]	Re[S ₂₂]	Im[S ₂₂]
27 MHz	0.8417	-0.0151	1.36E-004	8.63E-005	-4.0840	0.1272	0.9994	-0.0092
40 MHz	0.8424	-0.0276	1.42E-004	1.07E-004	-4.0840	0.2055	0.9994	-0.0135
80 MHz	0.8403	-0.0621	1.52E-004	1.83E-004	-4.0630	0.4338	0.9991	-0.0269
170 MHz	0.8273	-0.1344	1.86E-004	3.72E-003	-3.9550	0.9279	0.9977	-0.0571
315 MHz	0.7884	-0.2328	4.02E-004	7.04E-003	-3.5100	1.6990	0.9846	-0.1072
433 MHz	0.7492	-0.3405	1.51E-004	6.18E-003	-3.4700	1.9920	0.9839	-0.1439
868 MHz	0.5007	-0.5322	2.36E-004	1.06E-003	-1.6710	3.2230	0.9501	-0.2847
915 MHz	0.4714	-0.5440	1.94E-004	1.06E-003	-1.4690	3.2700	0.9451	-0.2995

Note: input and output of the LNA are connected to 50 Ω ports without matching elements

9.3 LNA Input Impedances in Transmit Mode

Mode	LNA off, Pin LNA is shorted				
Frequency	R_s	L_s	Frequency	R_s	L_s
27 MHz	33.5 Ω	0.6 nH	315 MHz	33.9 Ω	1.1 nH
40 MHz	33.5 Ω	0.8 nH	433 MHz	33.2 Ω	0.8 nH
80 MHz	33.4 Ω	1.1 nH	868 MHz	32.8 Ω	1.2 nH
170 MHz	33.5 Ω	1.2 nH	915 MHz	32.8 Ω	1.2 nH

PRELIMINARY

10 Package Dimensions

The “exposed pad” is not connected to internal ground, it should not be connected to the PCB.

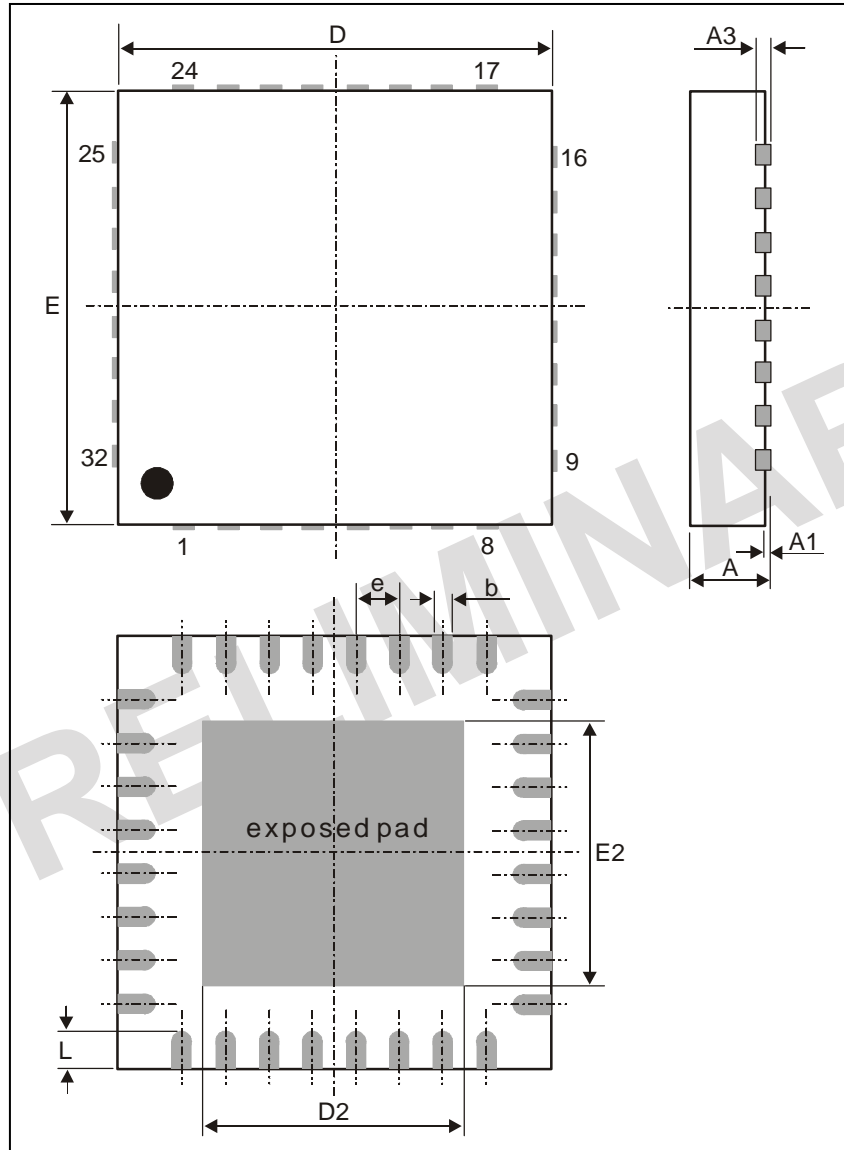


Fig. 20: 32L MLPQ 5x5 (Micro Leadframe Package Quad)

all Dimension in mm										
	D	E	D2	E2	A	A1	A3	L	e	b
min	4.75	4.75	3.00	3.00	0.80	0	0.20	0.3	0.50	0.18
max	5.25	5.25	3.25	3.25	1.00	0.05		0.5		0.30
all Dimension in inch										
min	0.187	0.187	0.118	0.118	0.0315	0	0.0079	0.0118	0.0197	0.0071
max	0.207	0.207	0.128	0.128	0.0393	0.002		0.0197		0.0118

11 Reliability Information

This Melexis device is classified and qualified regarding soldering technology, solderability and moisture sensitivity level, as defined in this specification, according to following test methods:

- IPC/JEDEC J-STD-020
Moisture/Reflow Sensitivity Classification For Nonhermetic Solid State Surface Mount Devices (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing (reflow profiles according to table 2)
- CECC00802
Standard Method For The Specification of Surface Mounting Components (SMDs) of Assessed Quality
- EIA/JEDEC JESD22-B106
Resistance to soldering temperature for through-hole mounted devices
- EN60749-15
Resistance to soldering temperature for through-hole mounted devices
- MIL 883 Method 2003 / EIA/JEDEC JESD22-B102
Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Based on Melexis commitment to environmental responsibility, European legislation (Directive on the Restriction of the Use of Certain Hazardous substances, RoHS) and customer requests, Melexis has installed a Roadmap to qualify their package families for lead free processes also.

Various lead free generic qualifications are running, current results on request.

For more information on manufacturability/solderability see quality page at our website:

<http://www.melexis.com/html/pdf/MLXleadfree-statement.pdf>

12 ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).

Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

13 Disclaimer

Devices sold by Melexis are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. Melexis makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Melexis reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with Melexis for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by Melexis for each application.

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PRELIMINARY

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Or for additional information contact Melexis Direct:

Europe and Japan:

Phone: +32 1367 0495

E-mail: sales_europe@melexis.com

All other locations:

Phone: +1 603 223 2362

E-mail: sales_usa@melexis.com

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